TECHNICAL MANUAL

DIRECT SUPPORT

AND

GENERAL SUPPORT

MAINTENANCE MANUAL

DRAGON MAINTENANCE SET

DEPARTMENT OF THE ARMY

MAY 1984

Technical Manual)
)
9-4935-677-34-2)

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, D.C., 15 May 1984

DIRECT SUPPORT AND GENERAL SUPPORT MAINTENANCE MANUAL DRAGON MAINTENANCE SET

LIST OF ILLUSTRATIONS

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CHAPTER 4

AN/TSM-128 SCHEMATIC DIAGRAMS

NOTE

This manual has been prepared primarily to provide the US Marine Corps with operator and equipment maintenance instructions for the DRAGON Maintenance Set (DMS) and will replace the following documents presently in use by the Marine Corps: TM 9-4935-481-14-1, dated 22 April 1977; TM 9-4935-481-14-2, dated 29 April 1977; TM 9-4935-481-14-3, dated 3 April 1981; and TM 9-4935-482-40, dated 5 May 1977; and all subsequent changes.

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R2	5
R3	4
R4	5
R5	4
R6	8
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P1	13
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R2	2
A2C1	2
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A2E3	2
* A2TB1	2
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A27R5	6
A27R6	8
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A27R8	8
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NOTES:

1. ALL VALUES IN OHMS AND MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. LOWER CASE LETTERS ARE SHOWN AS UNDERLINED UPPERCASE LETTERS.
3. NON-STANDARD ABBREVIATIONS:
   - 3.1 ABC-XXX MEANS DMS-D SELECTORS A, B, & C POSITION XXX.
   - 3.2 TTS MEANS TRACKER TEST SET.
   - 3.3 TX MEANS TIMING SIGNAL X.
4. PARTIAL REFERENCE DESIGNATION ARE SHOWN. FOR COMPLETE DESIGNATION. PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S). (PREFACE ALL DESIGNATIONS WITH A1 FIRST UNLESS OTHERWISE MARKED BY*)
5. SEE COMMERCIAL MANUAL AC/DC ELECTRONICS INC. #ACDC 96016 FOR SCHEMATIC OF PS1.
6. SEE COMMERCIAL MANUAL CONCORD INSTRUMENT DIVISION/SYSTRON DONNER CORPORATION MODEL 7460 MR FOR SCHEMATIC OF M1.
7. SEE COMMERCIAL MANUAL MONSANTO COMPANY COUNTER-TIMER MODEL 100C/101C FOR SCHEMATIC OF M2.
8. PS2 IS A SEALED UNIT. INTERNAL SCHEMATIC INFORMATION IS PROPRIETARY.
9. ALL WAFER SWITCH PIN NUMBERS ARE MARKED ON THE DECKS. DECK NUMBERS ARE IDENTIFIED BY BEGINNING WITH FIRST ALPHA OR NUMERIC DIGIT AT THE KNOB END. OTHER SWITCH PINS ARE IDENTIFIED AS SHOWN BELOW.

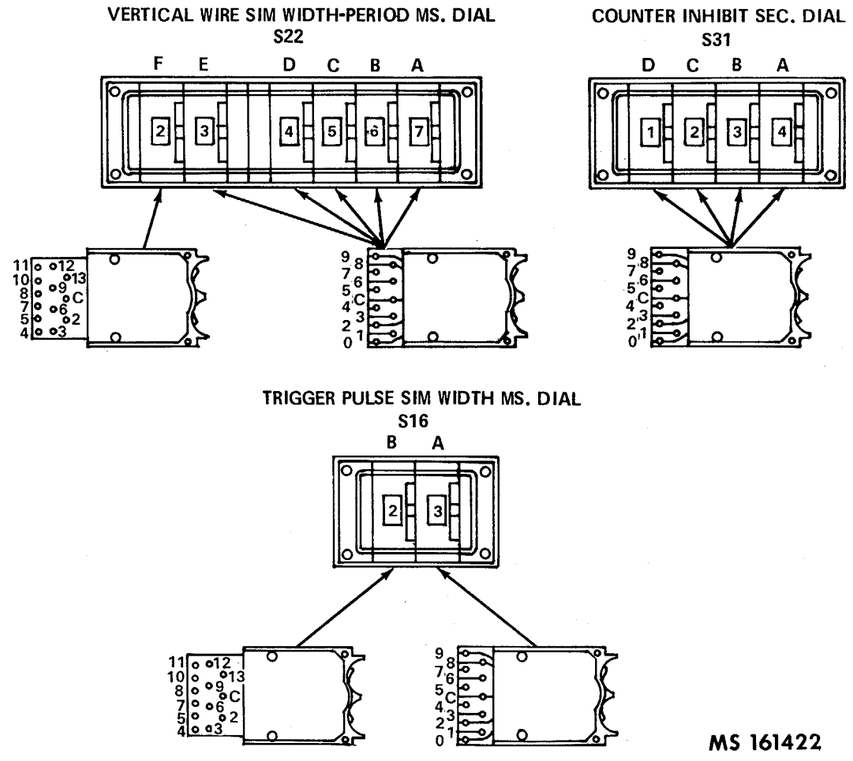

Figure 4-1. DMS-D - SCHEMATIC DIAGRAM (sheet 1 of 30)

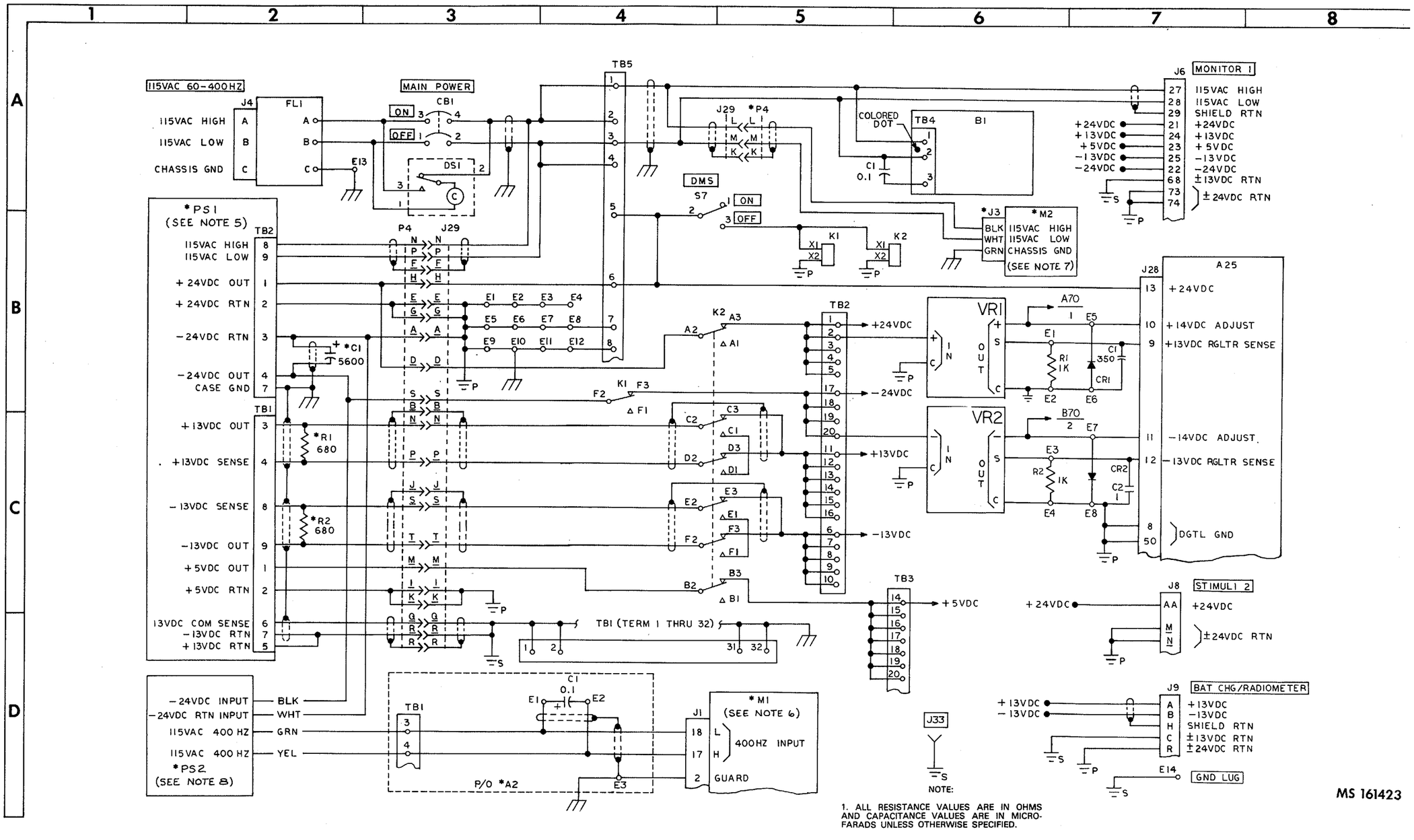

Figure 4-1. DMS-D - schematic diagram (sheet 2 of 30)

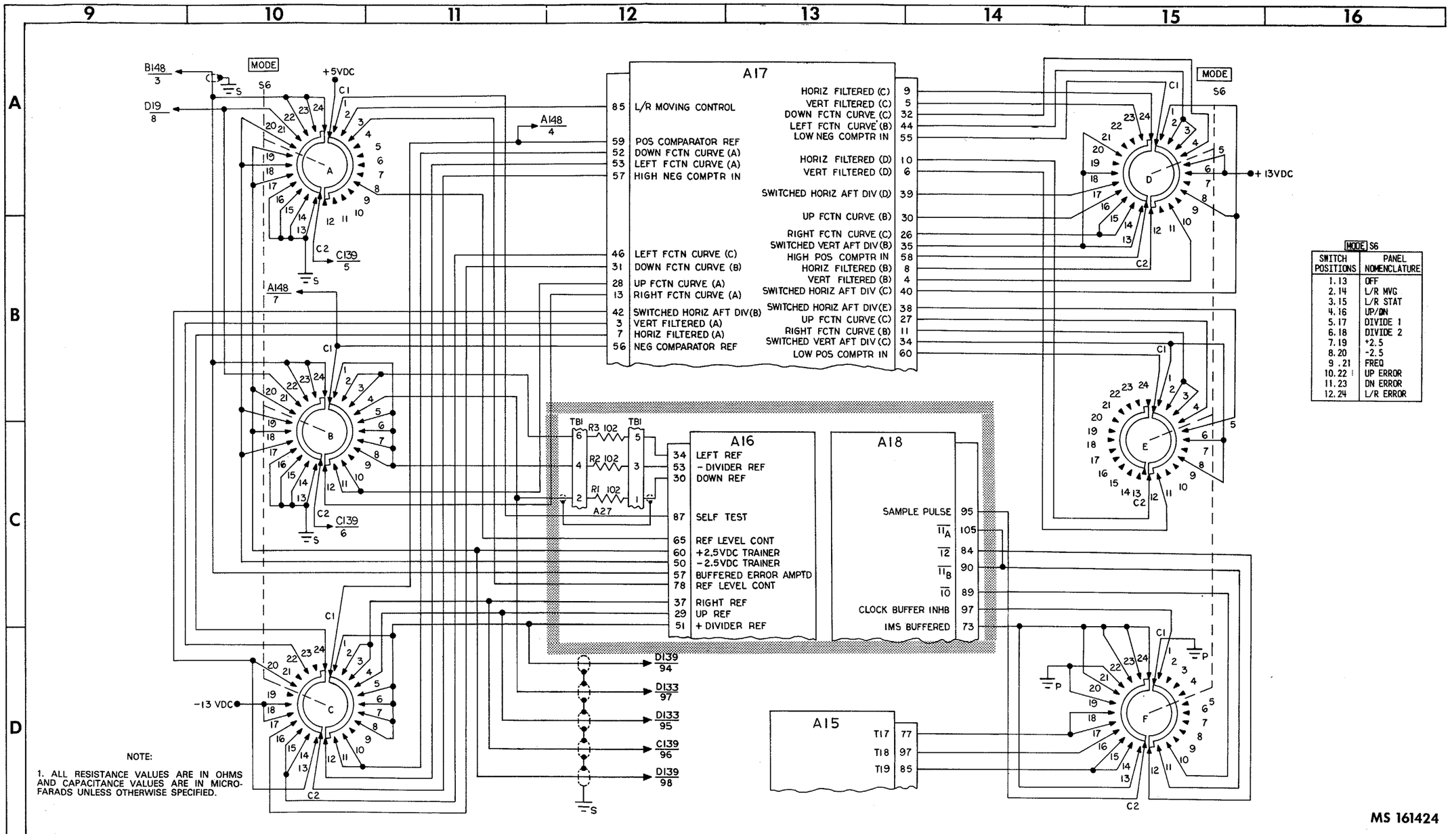

Figure 4-1. DMS-D - schematic diagram (sheet 3 of 30)

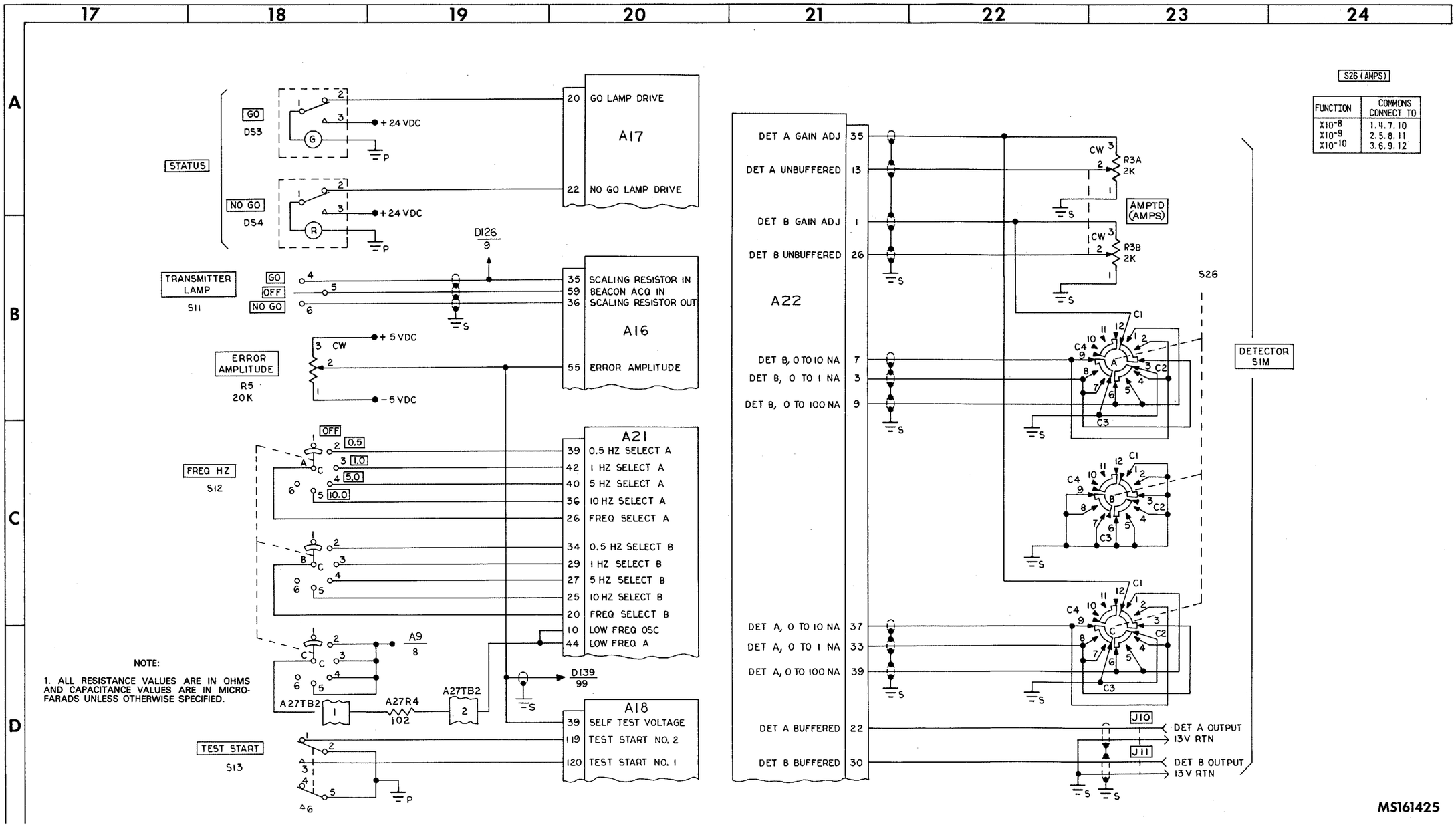

Figure 4-1. DMS-D - schematic diagram (sheet 4 of 30)

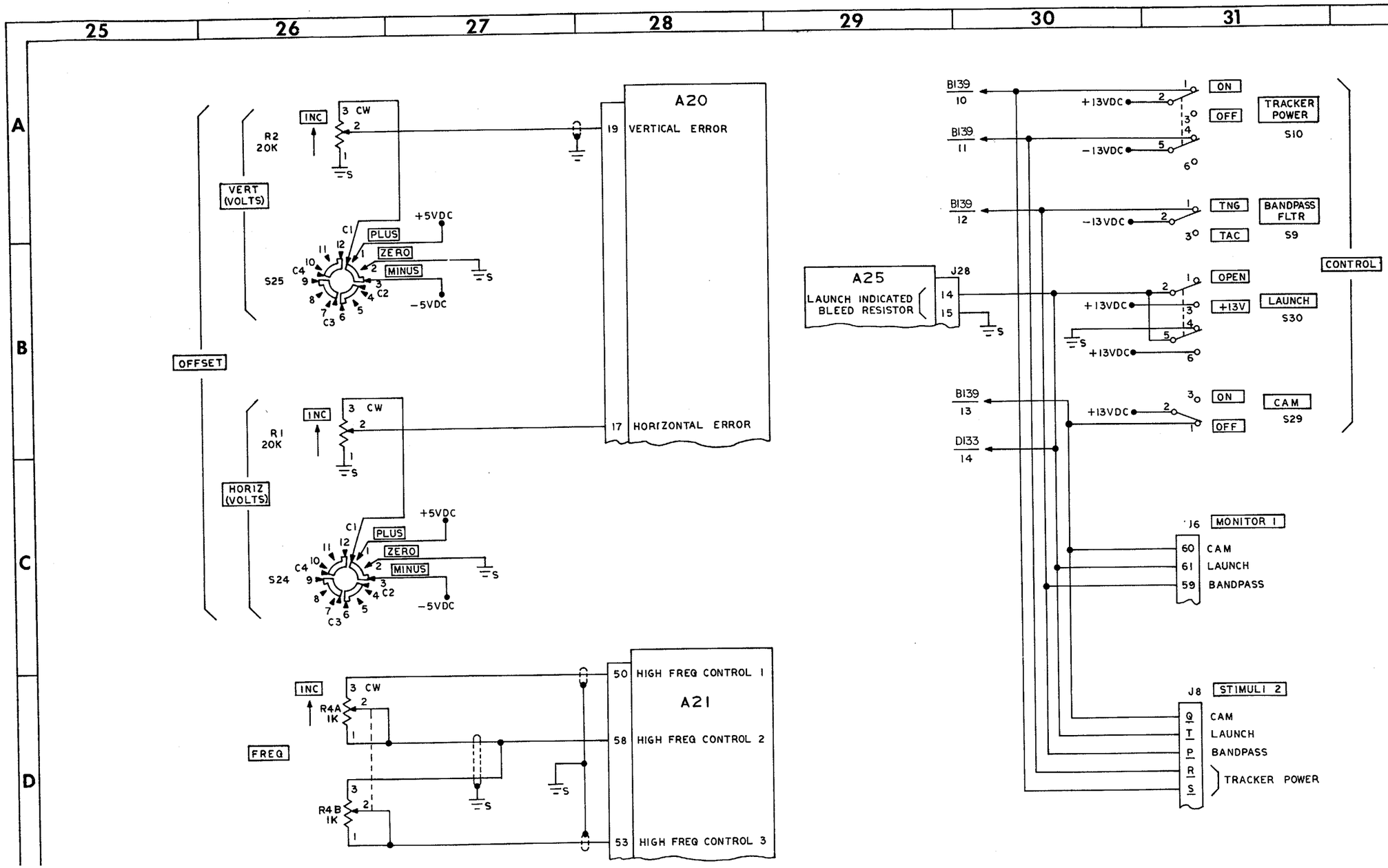

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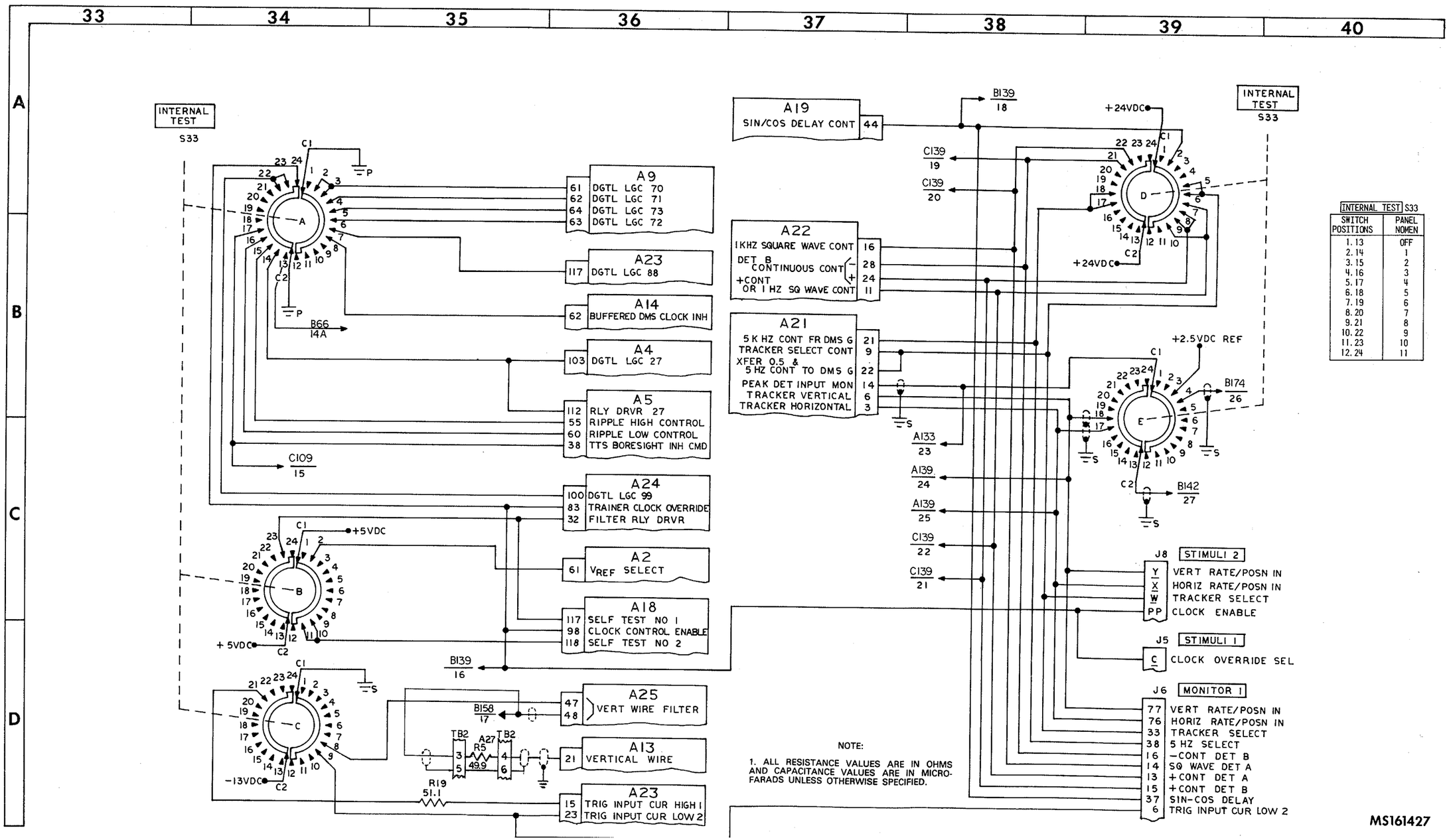
Figure 4-1. DMS-D - schematic diagram (sheet 5 of 30)



INTERNAL TEST S33

SWITCH POSITIONS	PANEL NOMEN
1, 13	OFF
2, 14	1
3, 15	2
4, 16	3
5, 17	4
6, 18	5
7, 19	6
8, 20	7
9, 21	8
10, 22	9
11, 23	10
12, 24	11

Figure 4-1. DMS-D - schematic diagram (sheet 6 of 30)

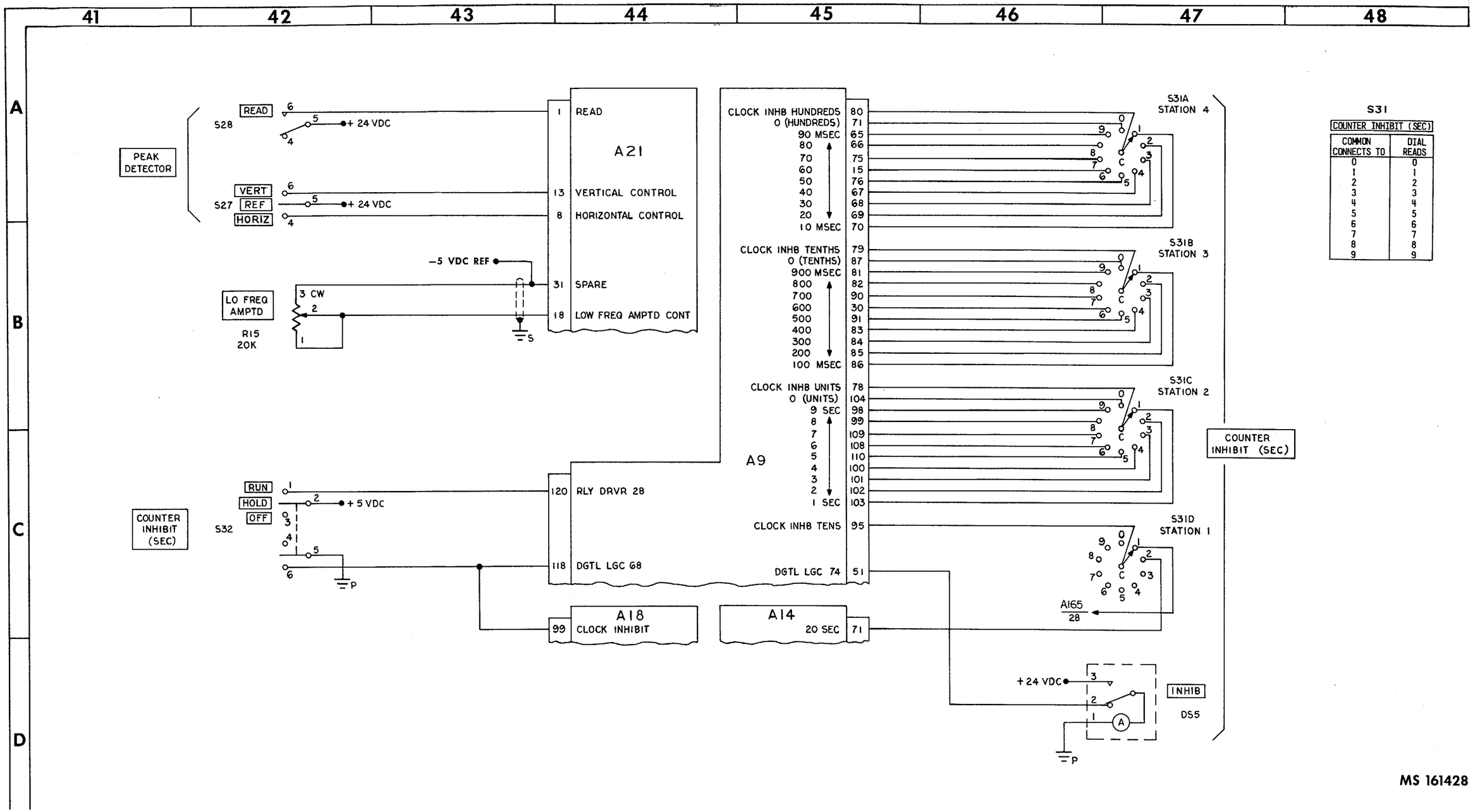


Figure 4-1. DMS-D - schematic diagram
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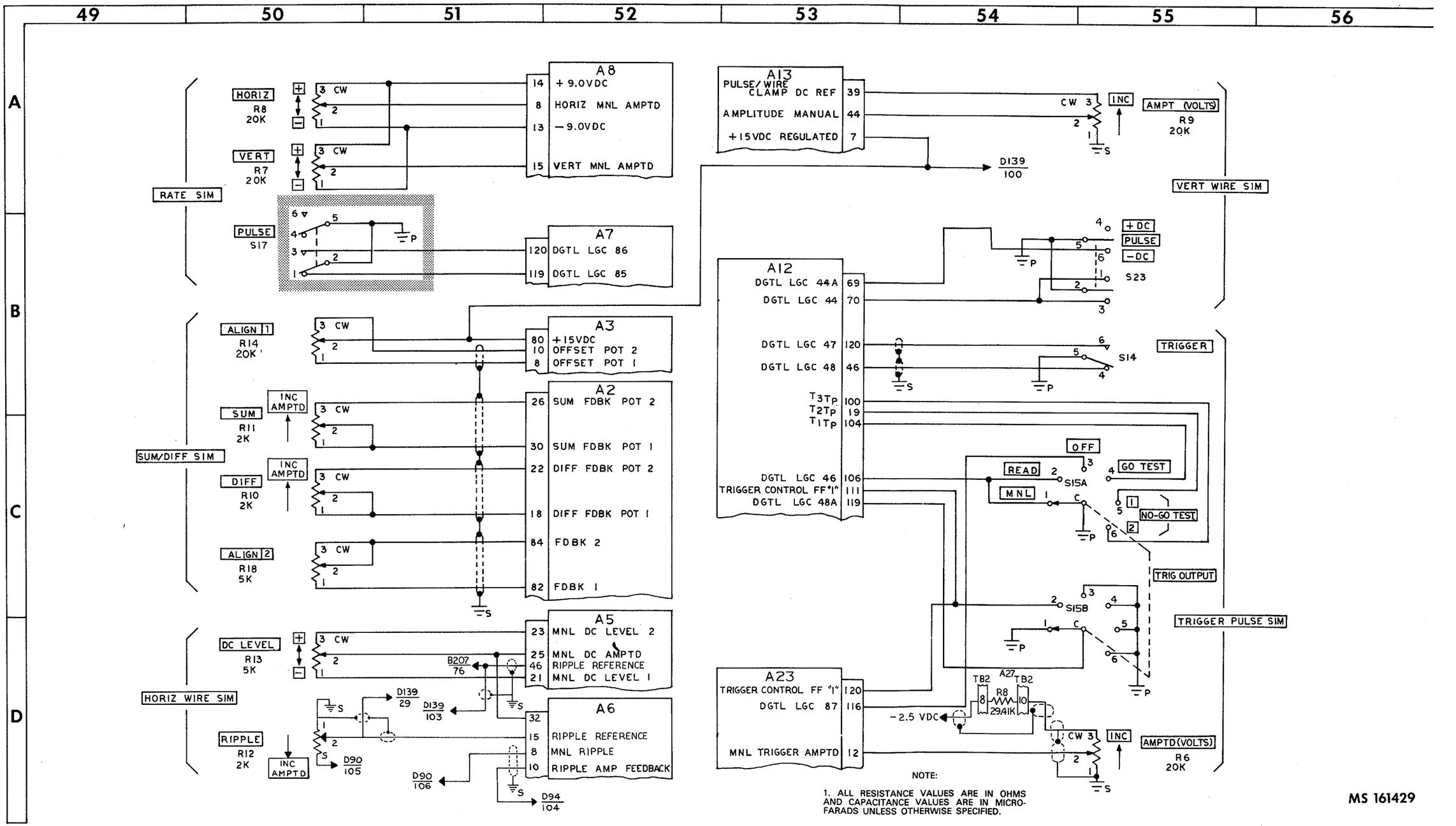
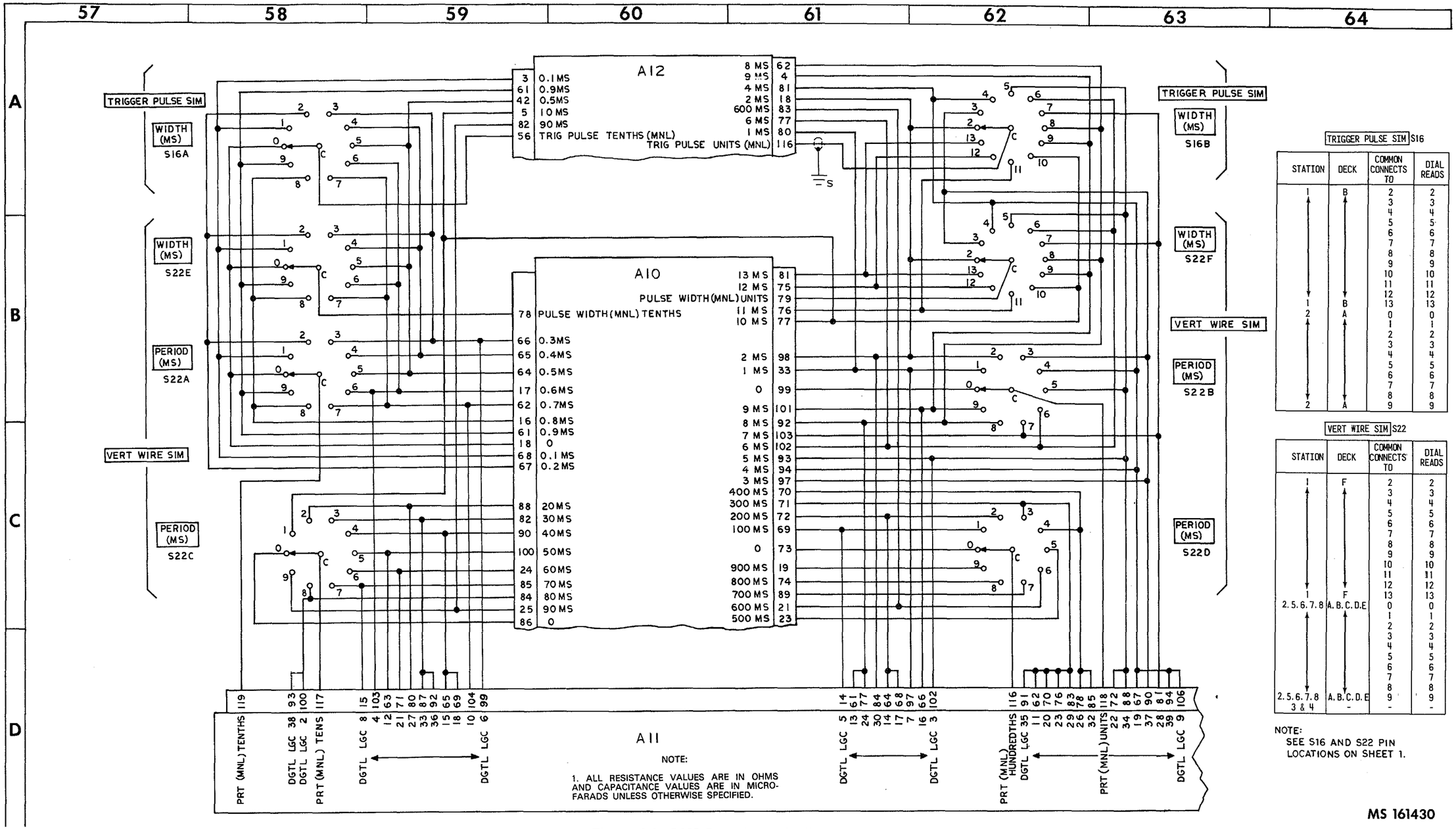


Figure 4-1. DMS-D - schematic diagram (sheet 8 of 30)



TRIGGER PULSE SIM S16

STATION	DECK	COMMON CONNECTS TO	DIAL READS
1	B	2	2
		3	3
		4	4
		5	5
		6	6
		7	7
		8	8
		9	9
		10	10
		11	11
		12	12
1	B	13	13
2	A	0	0
		1	1
		2	2
		3	3
		4	4
		5	5
		6	6
		7	7
		8	8
2	A	9	9

VERT WIRE SIM S22

STATION	DECK	COMMON CONNECTS TO	DIAL READS
1	F	2	2
		3	3
		4	4
		5	5
		6	6
		7	7
		8	8
		9	9
		10	10
		11	11
		12	12
1	F	13	13
2. 5. 6. 7. 8	A. B. C. D. E	0	0
		1	1
		2	2
		3	3
		4	4
		5	5
		6	6
		7	7
		8	8
2. 5. 6. 7. 8 3 & 4	A. B. C. D. E	9	9
		-	-

NOTE:
SEE S16 AND S22 PIN LOCATIONS ON SHEET 1.

MS 161430

Figure 4-1. DMS-D - schematic diagram (sheet 9 of 30)

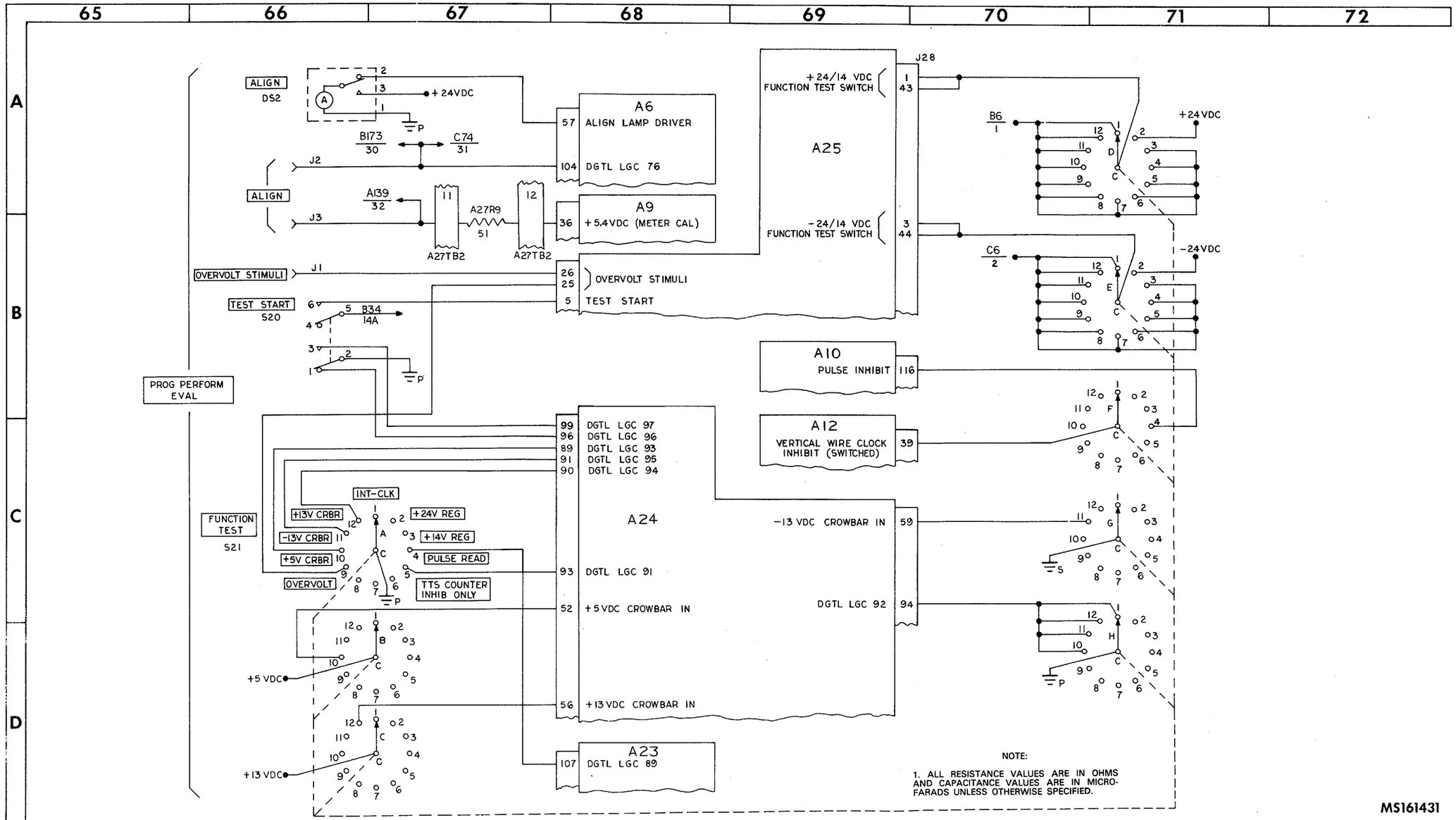


Figure 4-1. DMS-D - schematic diagram (sheet 10 of 30)

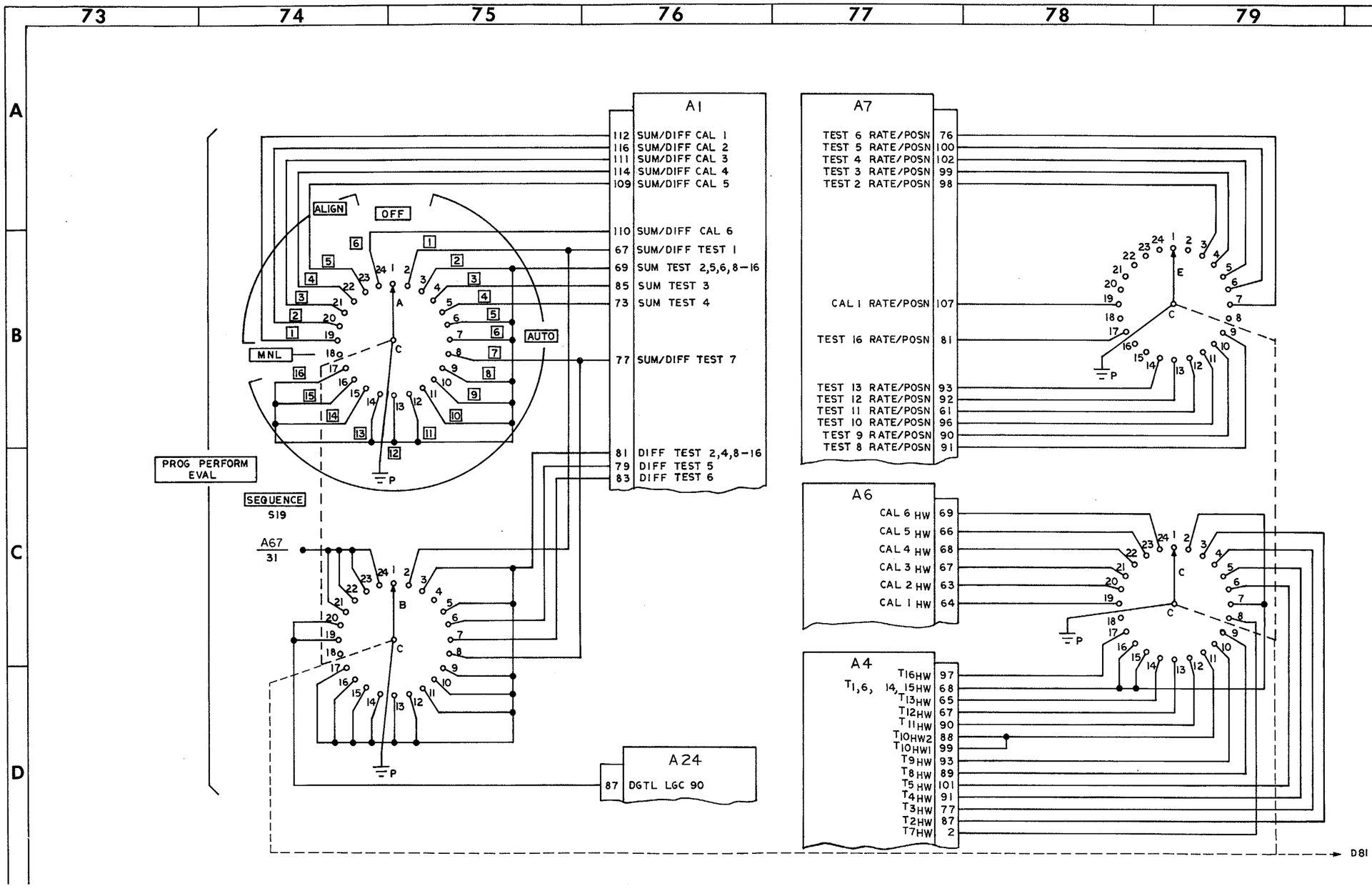


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Figure 4-1. DMS-D - schematic diagram (sheet 11 of 30)

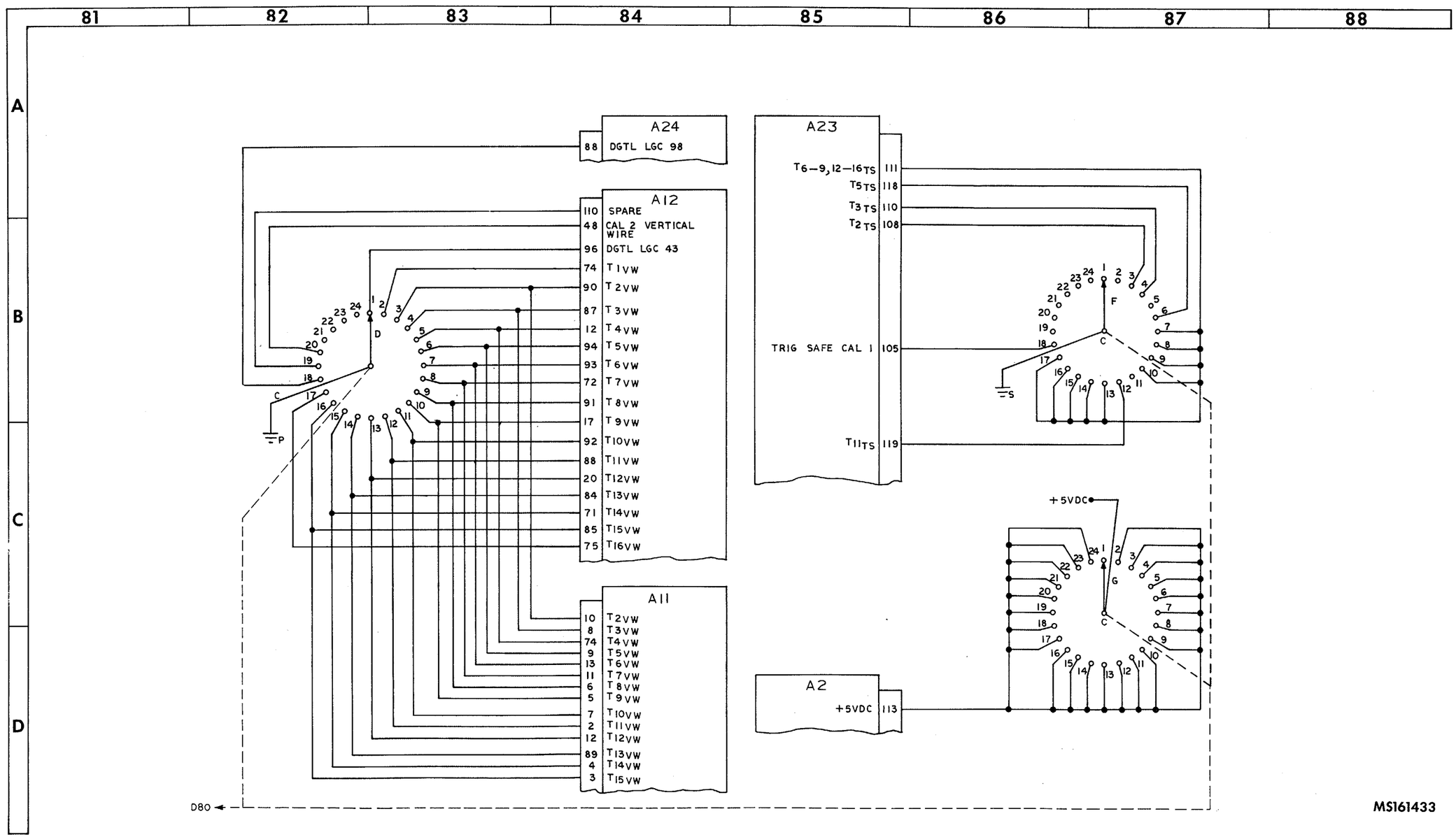
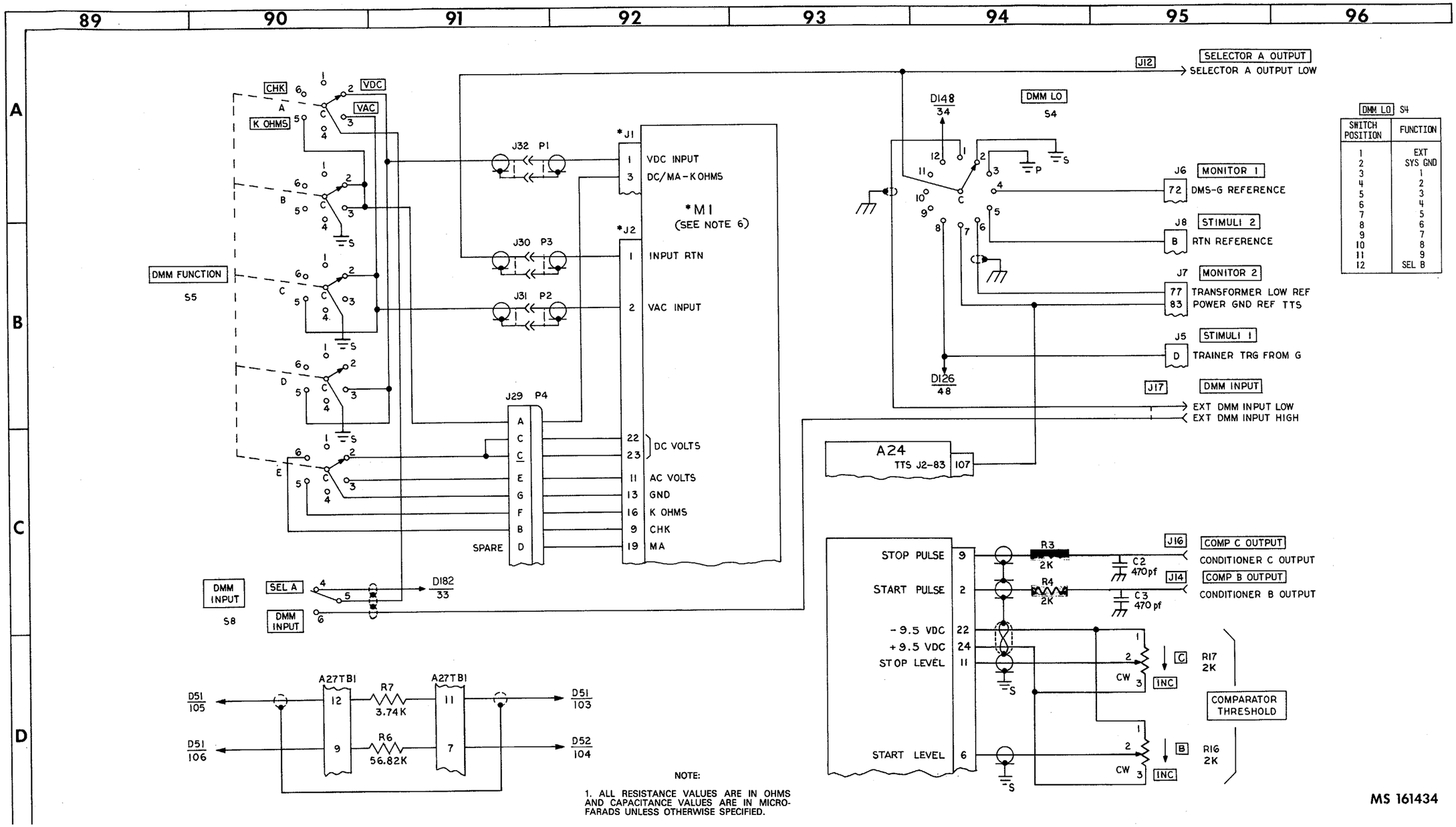


Figure 4-1 . DMS-D - schematic diagram (sheet 12 of 30)



NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

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Figure 4-1 . DMS-D - schematic diagram (sheet 13 of 30)

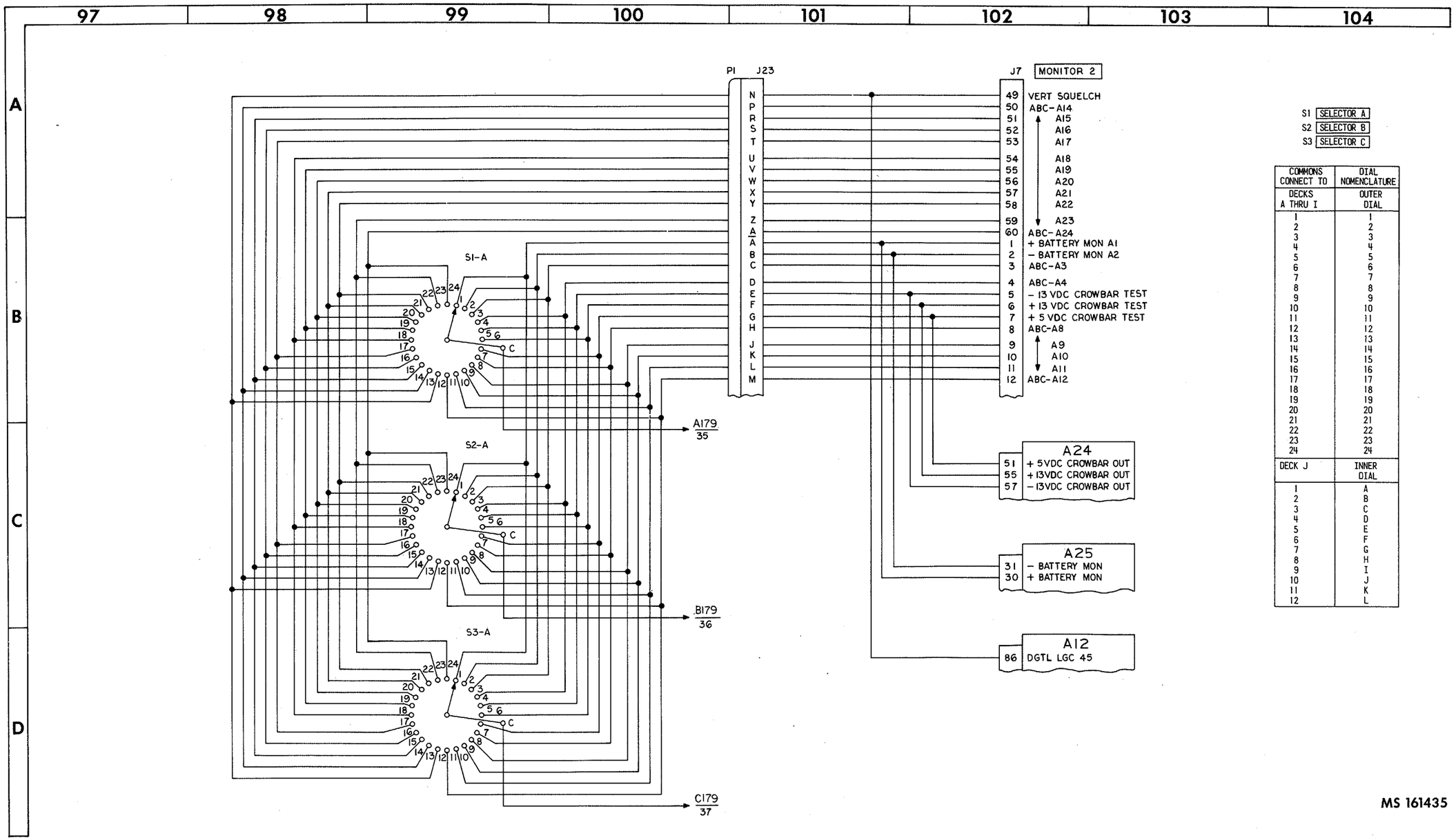
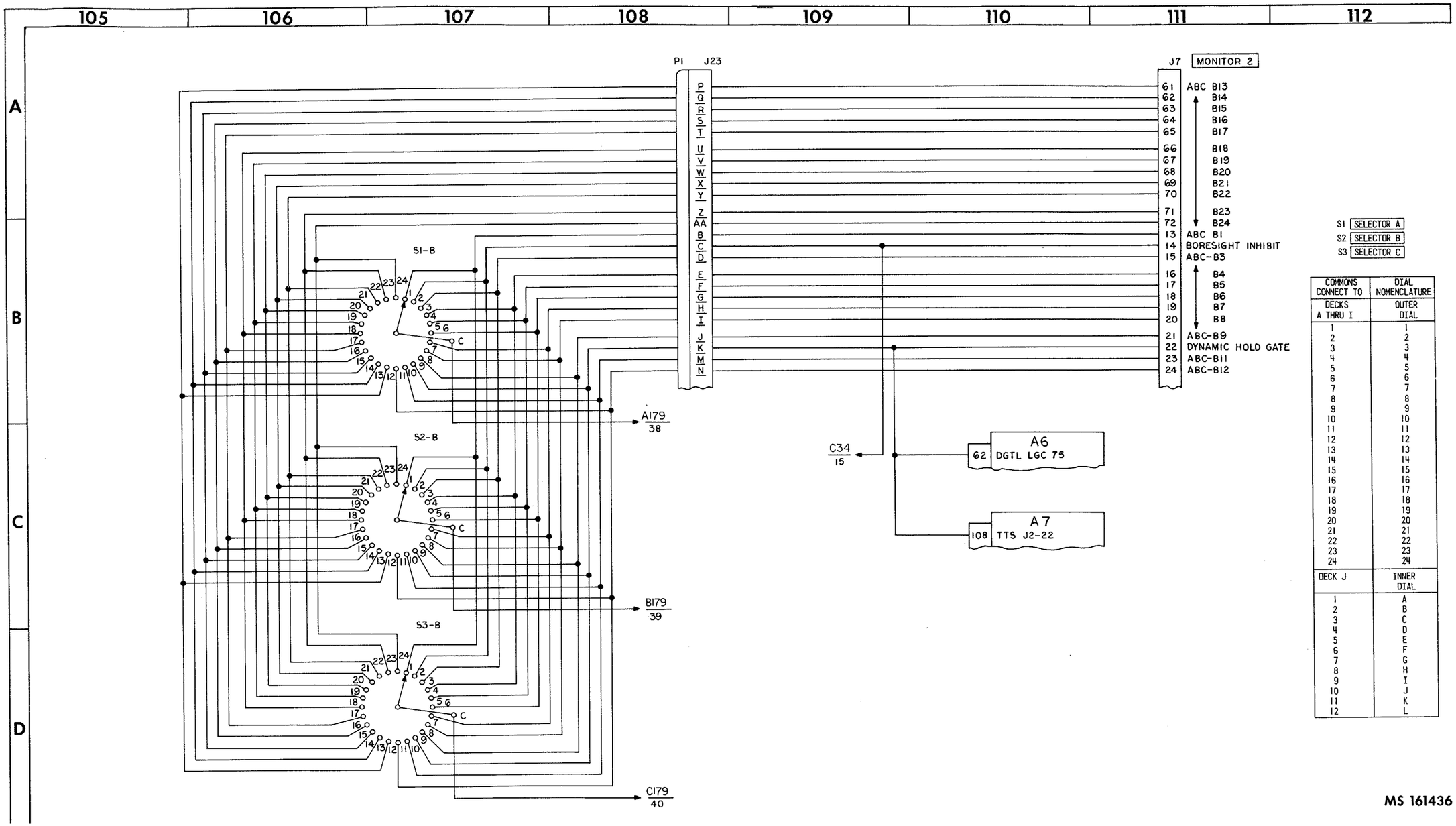
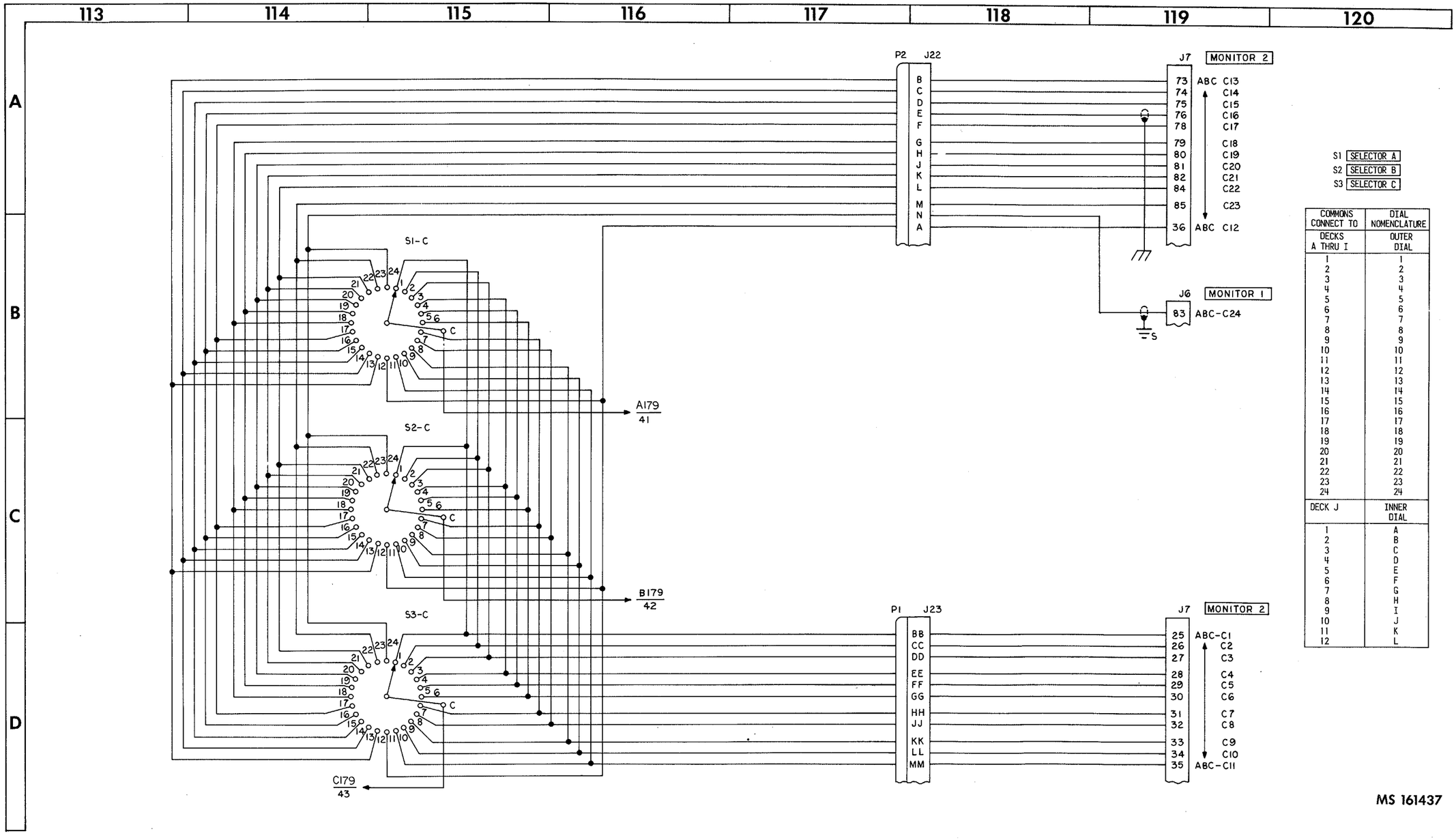


Figure 4-1. DMS-D - schematic diagram (sheet 14 of 30)



COMMONS CONNECT TO DECKS A THRU I	DIAL NOMENCLATURE OUTER DIAL
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	13
14	14
15	15
16	16
17	17
18	18
19	19
20	20
21	21
22	22
23	23
24	24
DECK J	INNER DIAL
1	A
2	B
3	C
4	D
5	E
6	F
7	G
8	H
9	I
10	J
11	K
12	L

Figure 4-1. DMS-D - schematic diagram (sheet 15 of 30)



COMMONS CONNECT TO DECKS A THRU I	DIAL NOMENCLATURE OUTER DIAL
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	13
14	14
15	15
16	16
17	17
18	18
19	19
20	20
21	21
22	22
23	23
24	24
DECK J	INNER DIAL
1	A
2	B
3	C
4	D
5	E
6	F
7	G
8	H
9	I
10	J
11	K
12	L

Figure 4-1. DMS-D - schematic diagram (sheet 16 of 30)

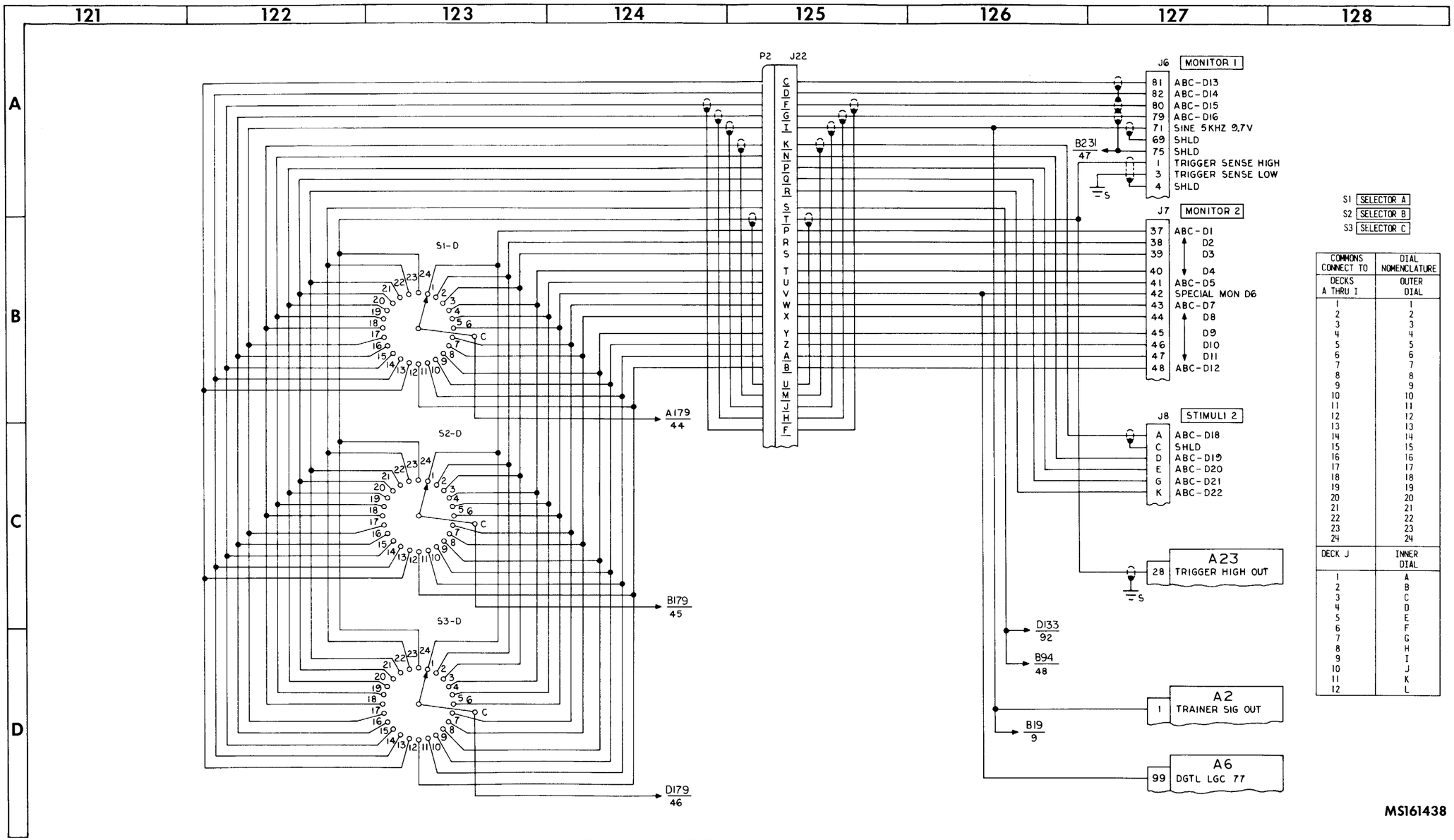
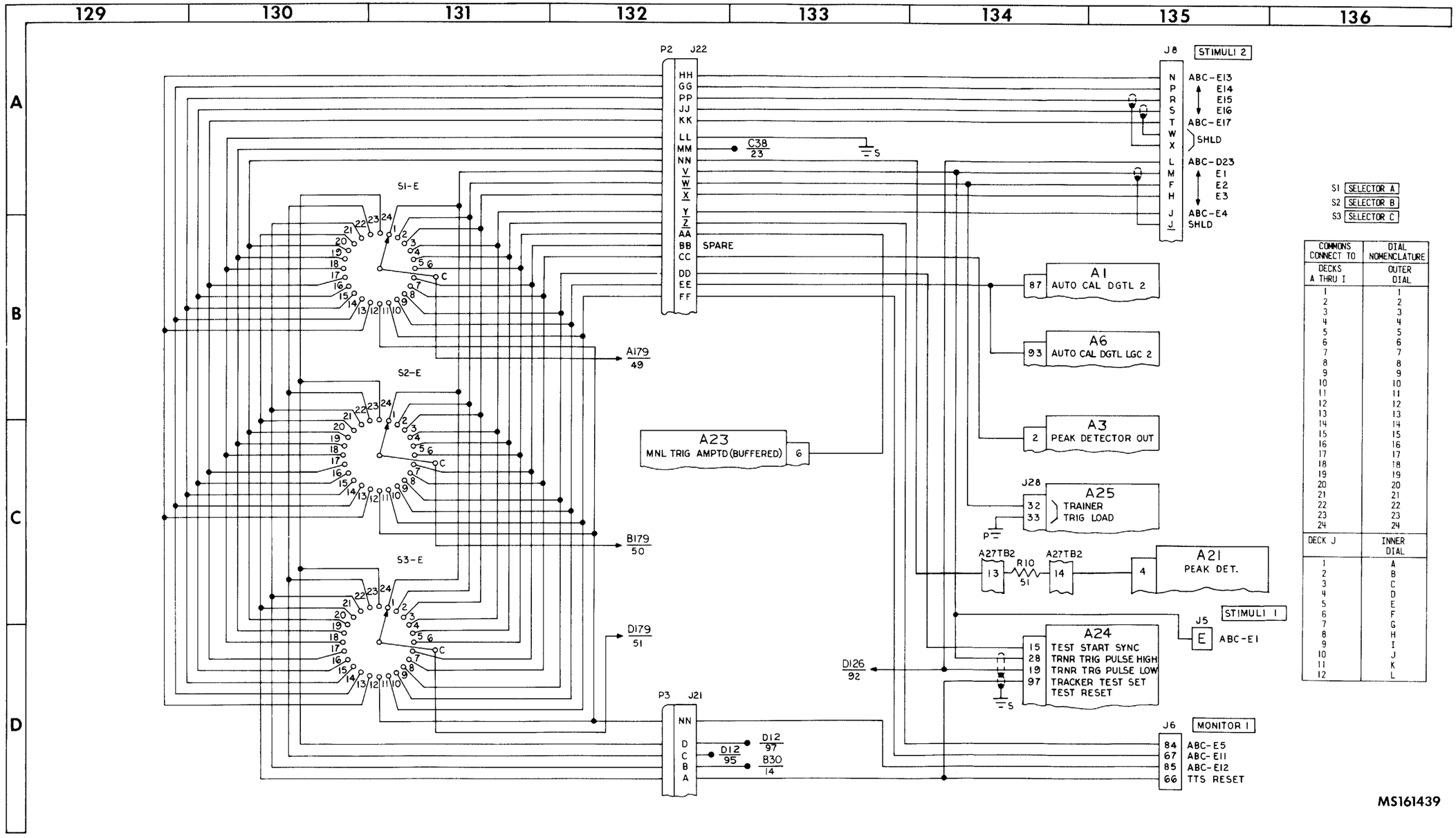


Figure 4-1. DMS-D - schematic diagram (sheet 17 of 30)



COMMONS CONNECT TO	DIAL NOMENCLATURE
DECKS A THRU I	OUTER DIAL
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	13
14	14
15	15
16	16
17	17
18	18
19	19
20	20
21	21
22	22
23	23
24	24
DECK J	INNER DIAL
1	A
2	B
3	C
4	D
5	E
6	F
7	G
8	H
9	I
10	J
11	K
12	L

Figure 4-1 DMS-D- schematic diagram (sheet 18 of 30)

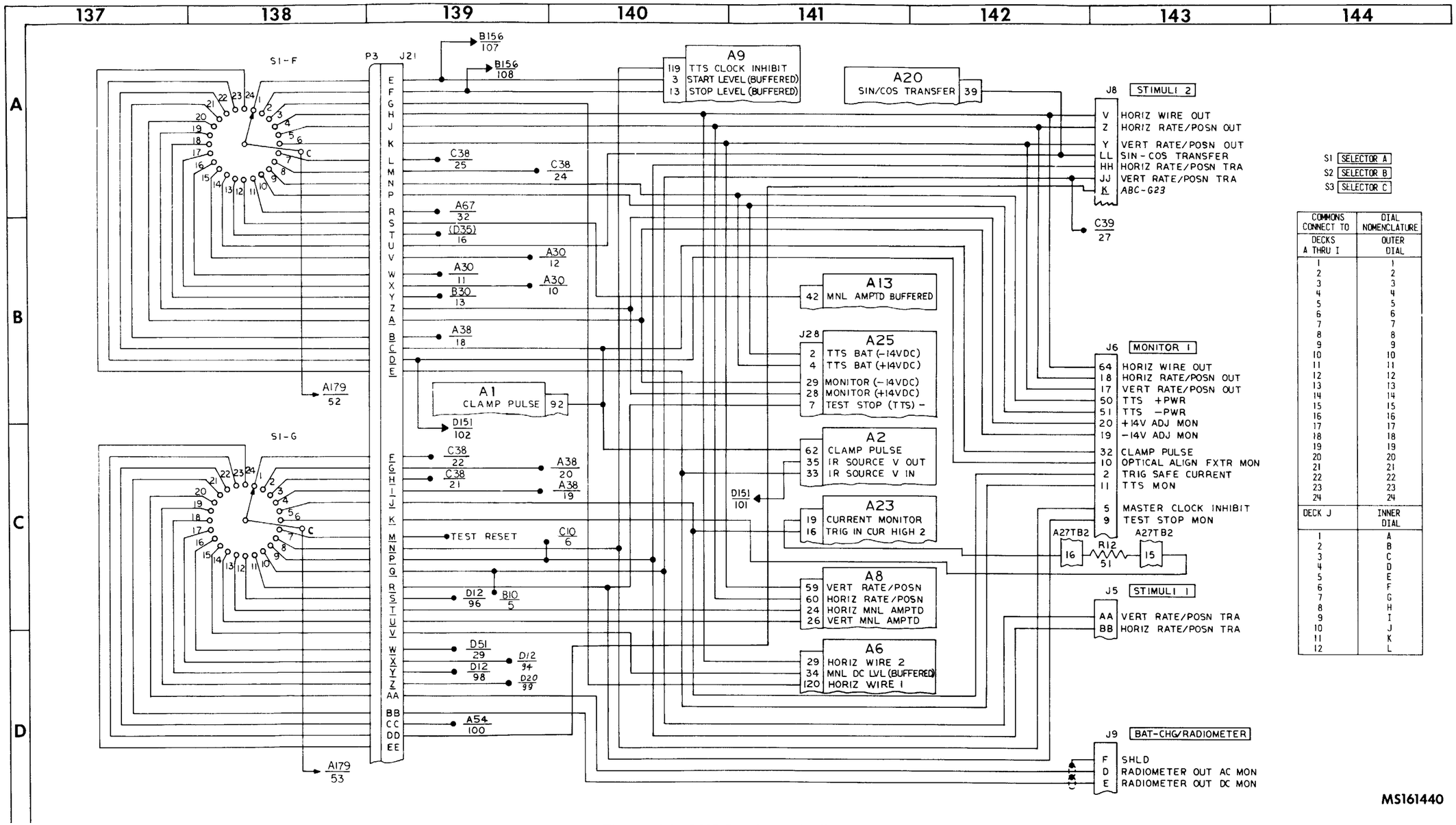


Figure 4-1. DMS-D-schematic diagram (sheet 19 of 30)

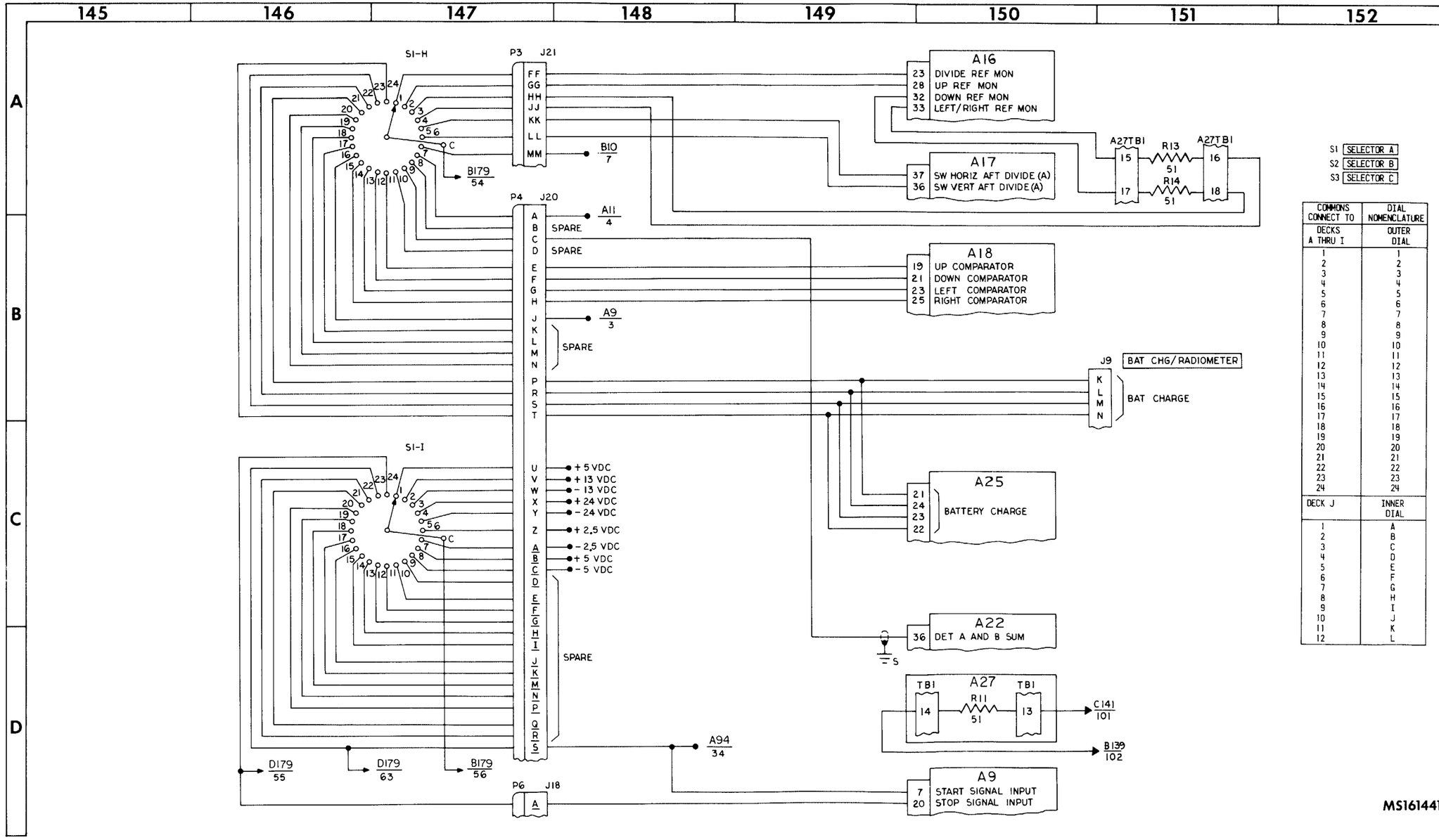


Figure 4-1. DMS-D-schematic diagram (sheet 20 of 30)

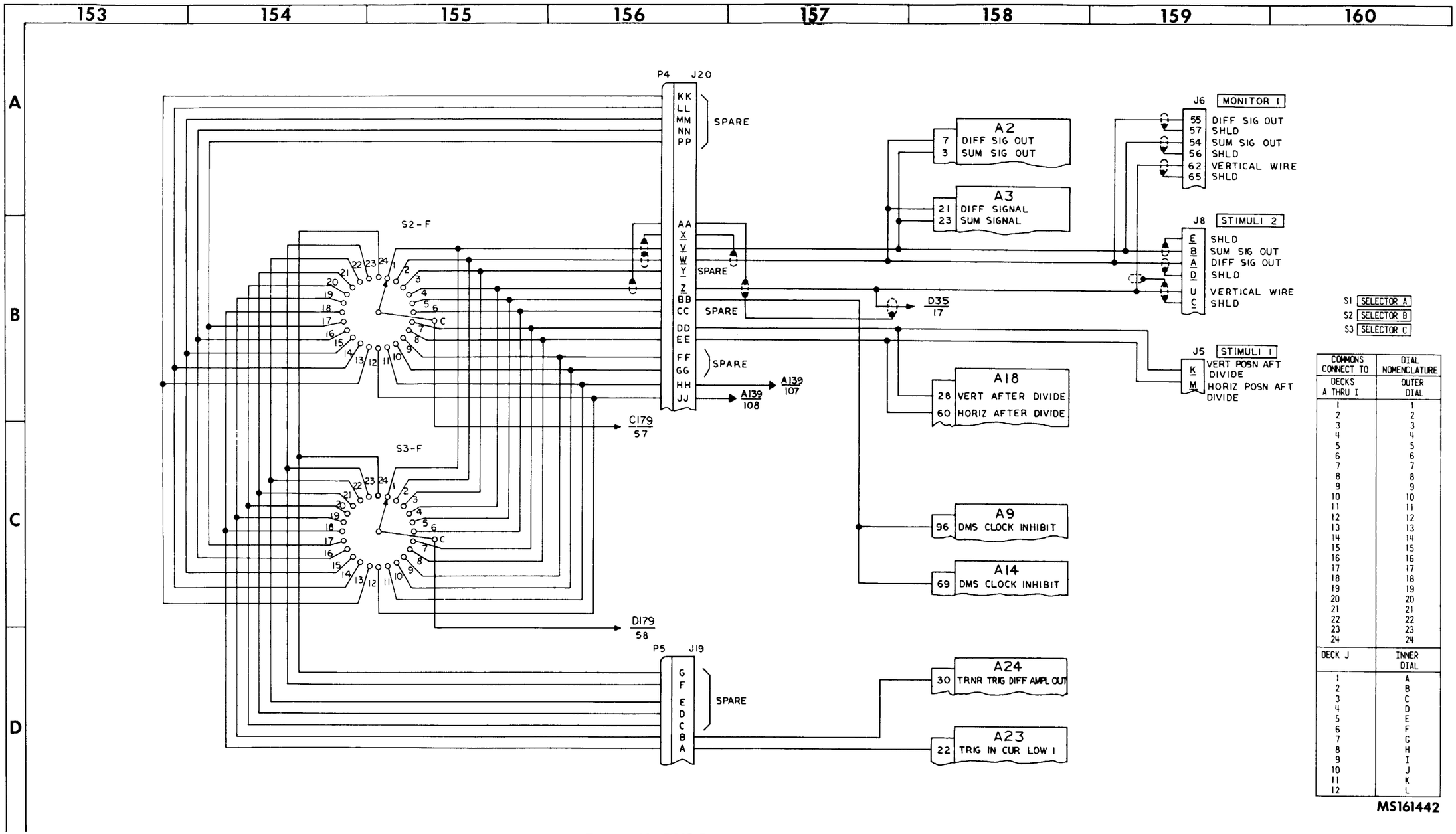


Figure 41. DMS-D- schematic diagram (sheet 21 of 30)

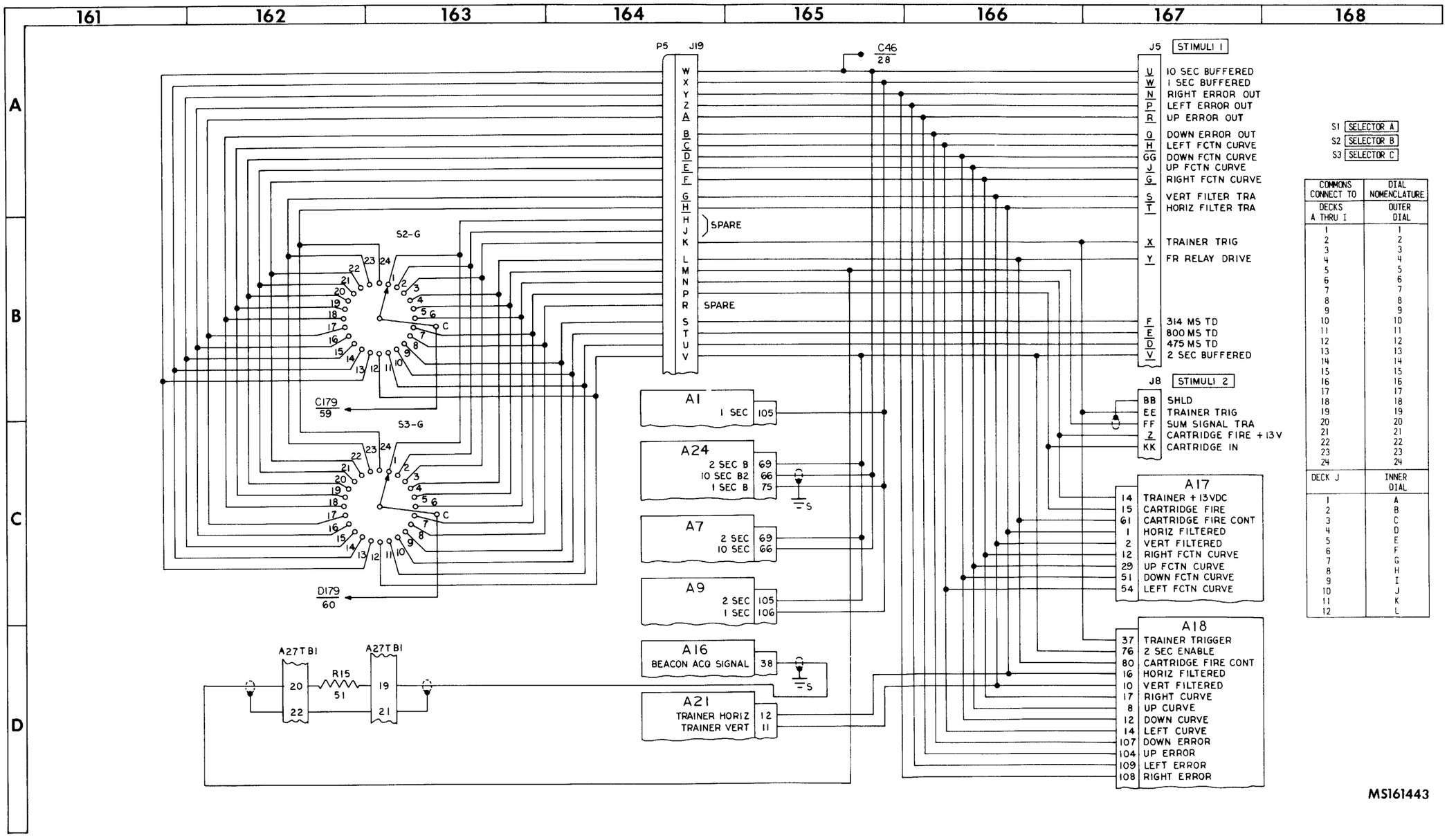
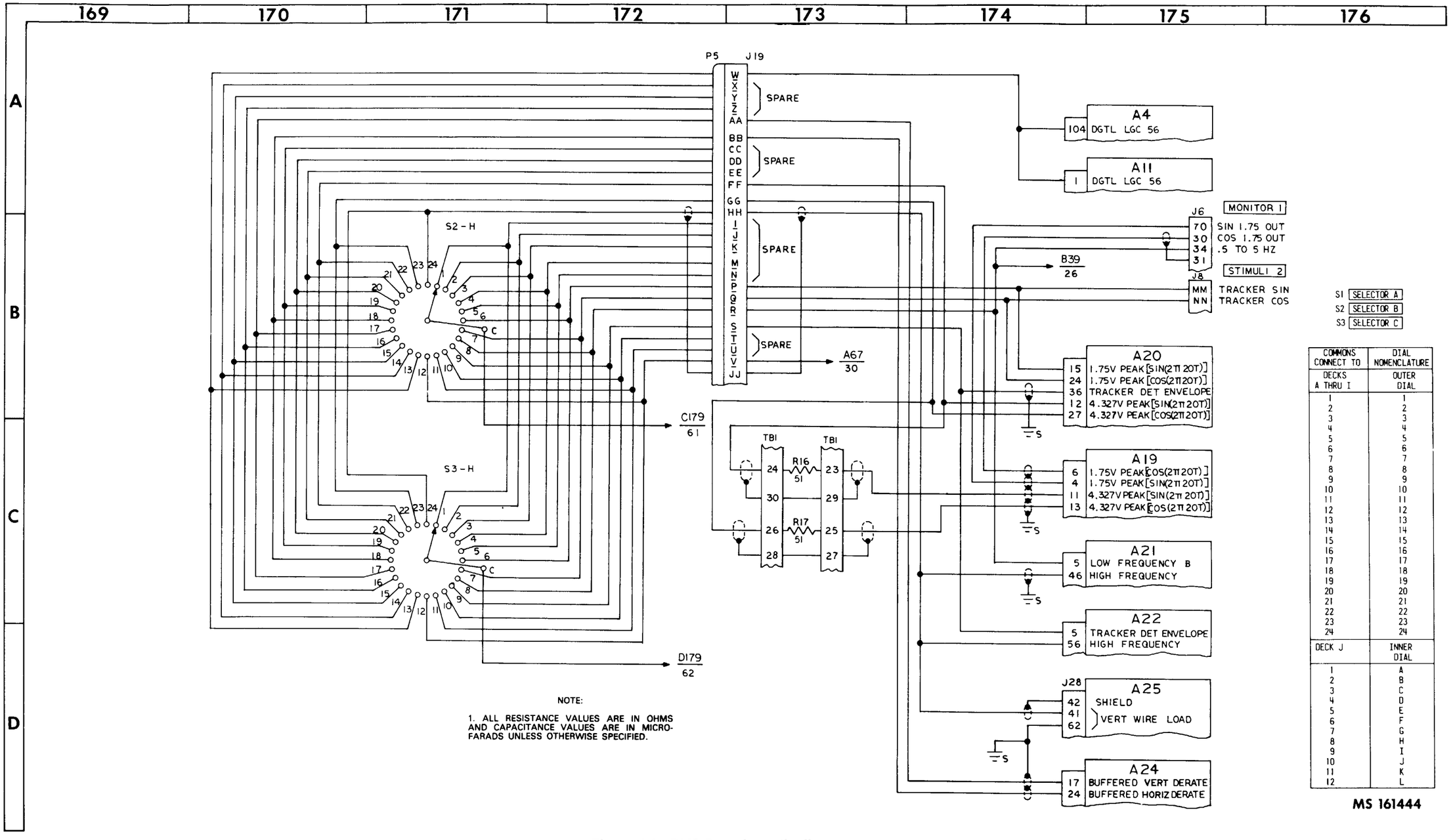


Figure 4-1. DMS-D- schematic diagram (sheet 22 of 30)



NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICRO-FARADS UNLESS OTHERWISE SPECIFIED.

Figure 4-1. DMS-D - schematic diagram (sheet 23 of 30)

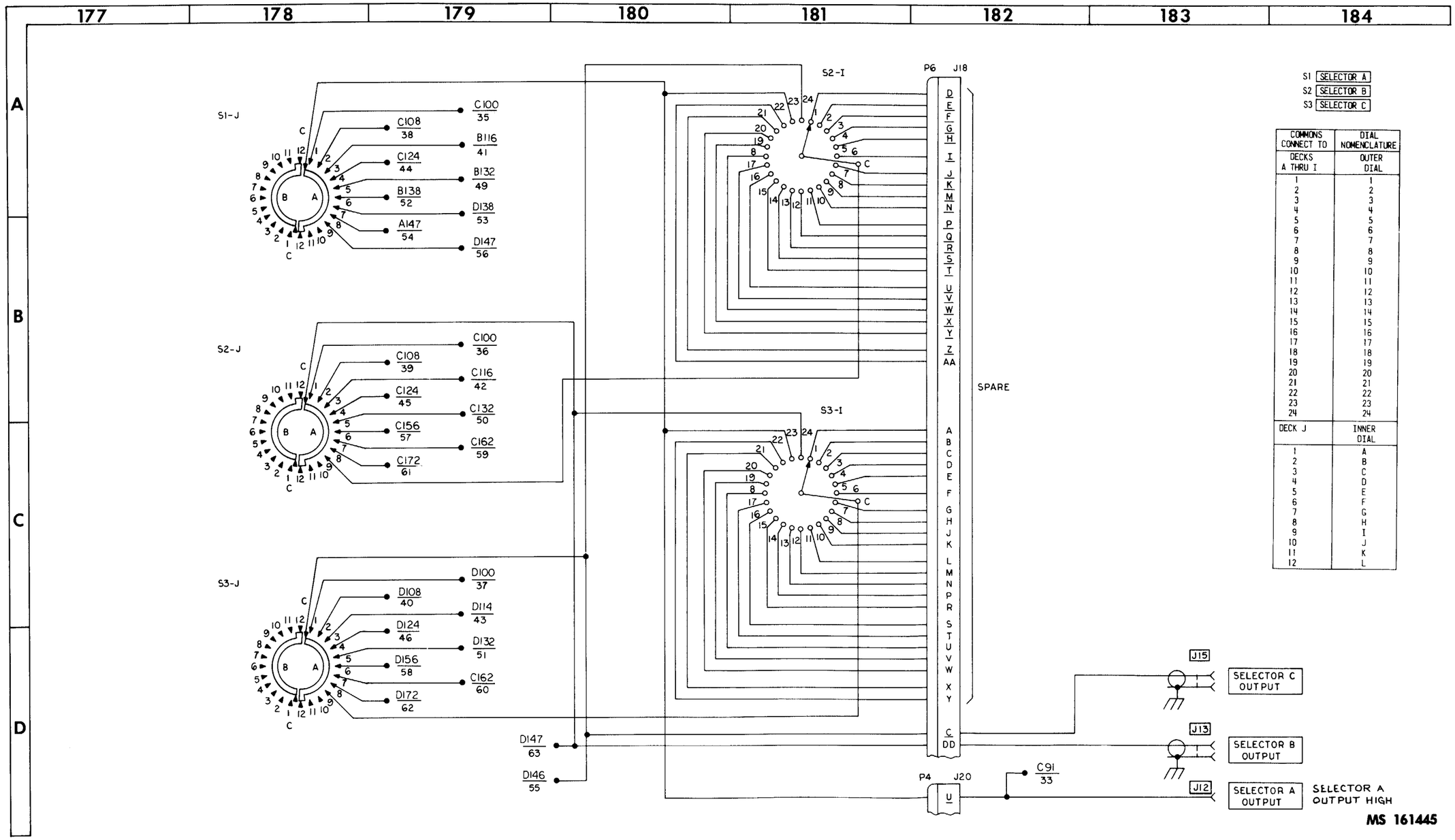


Figure 4-1. DMS-D - schematic diagram (sheet 24 of 30)

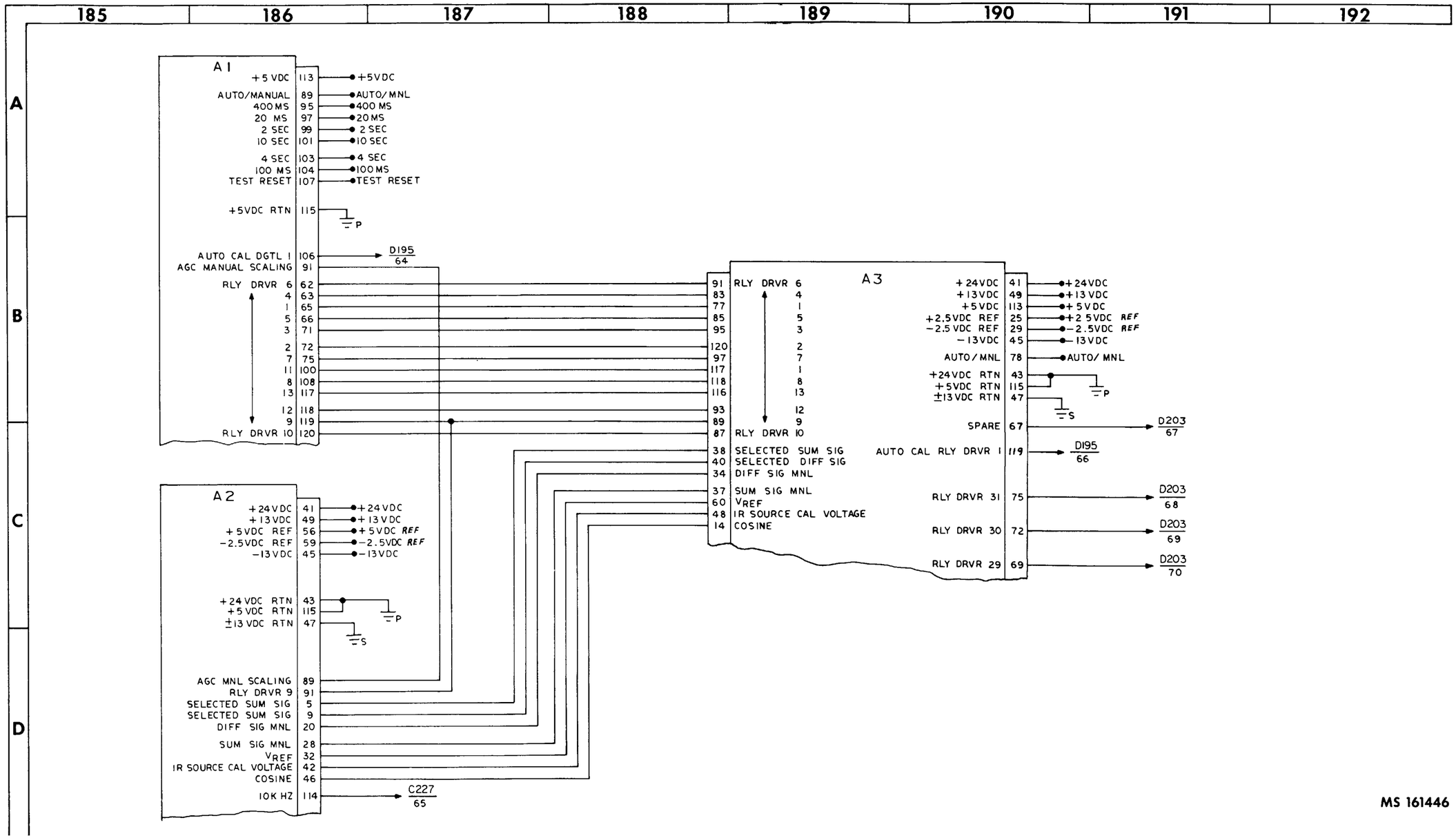


figure 4-1. DMS-D -schematic diagram
(sheet 25 of 30)

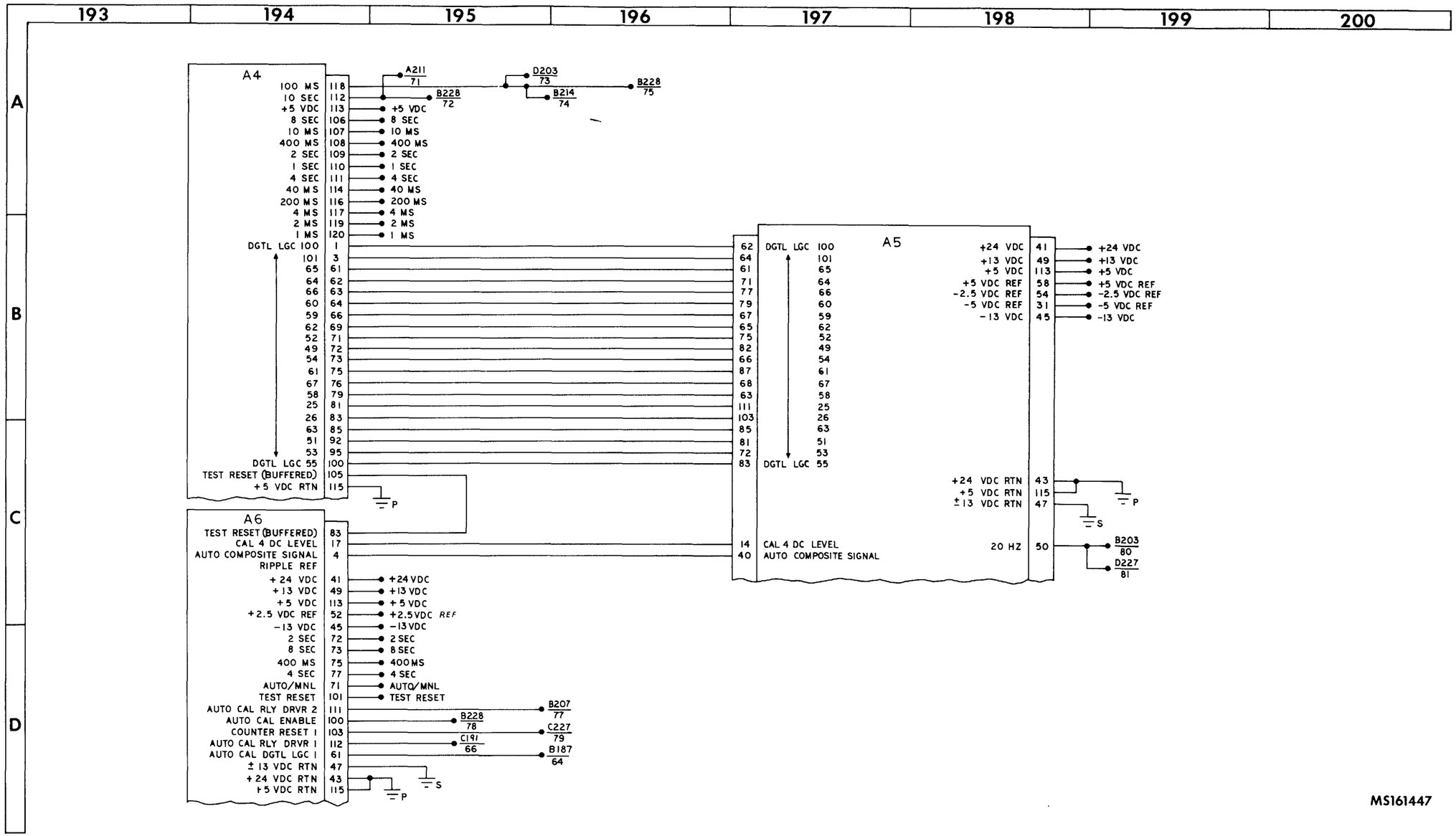
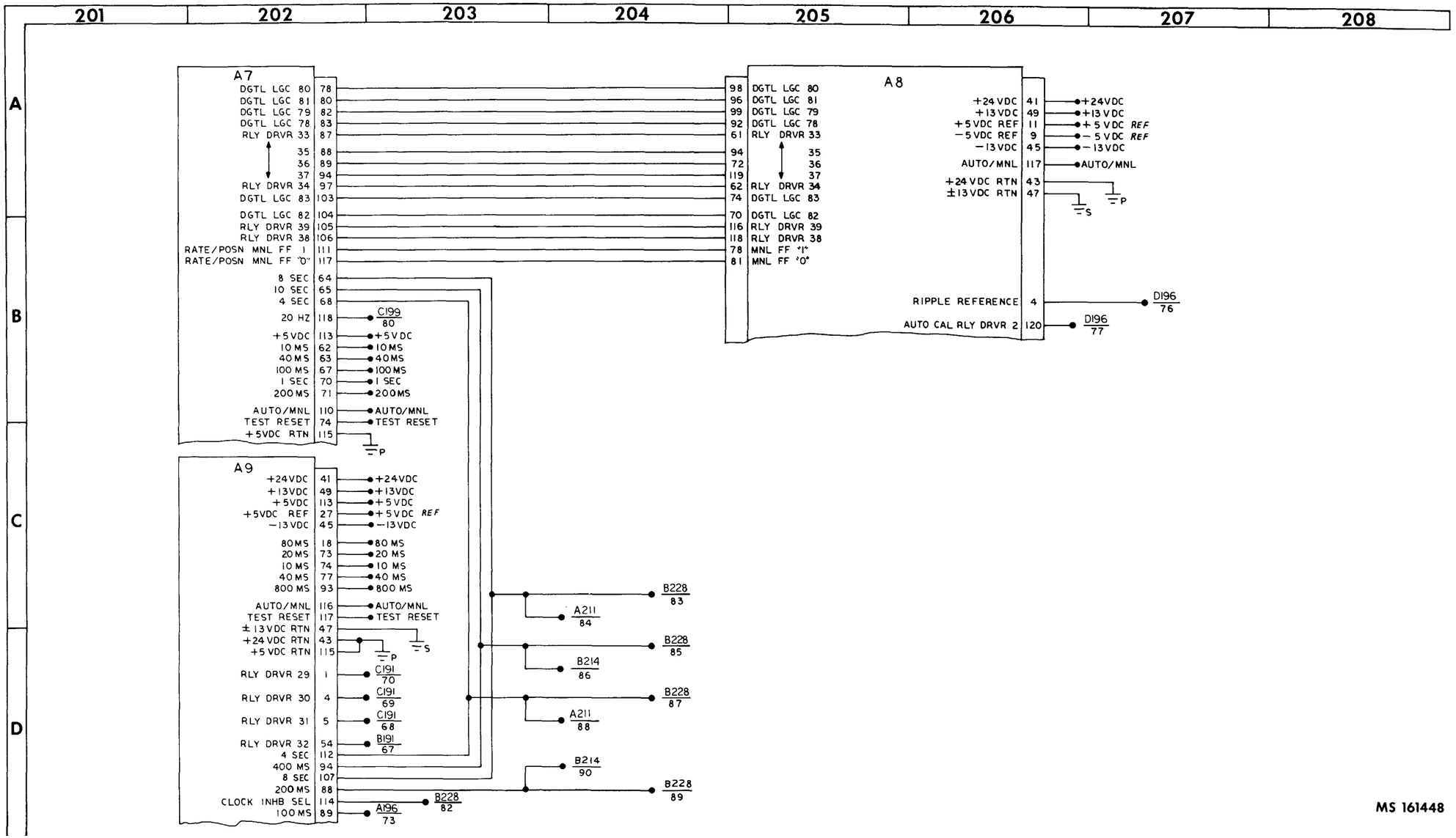
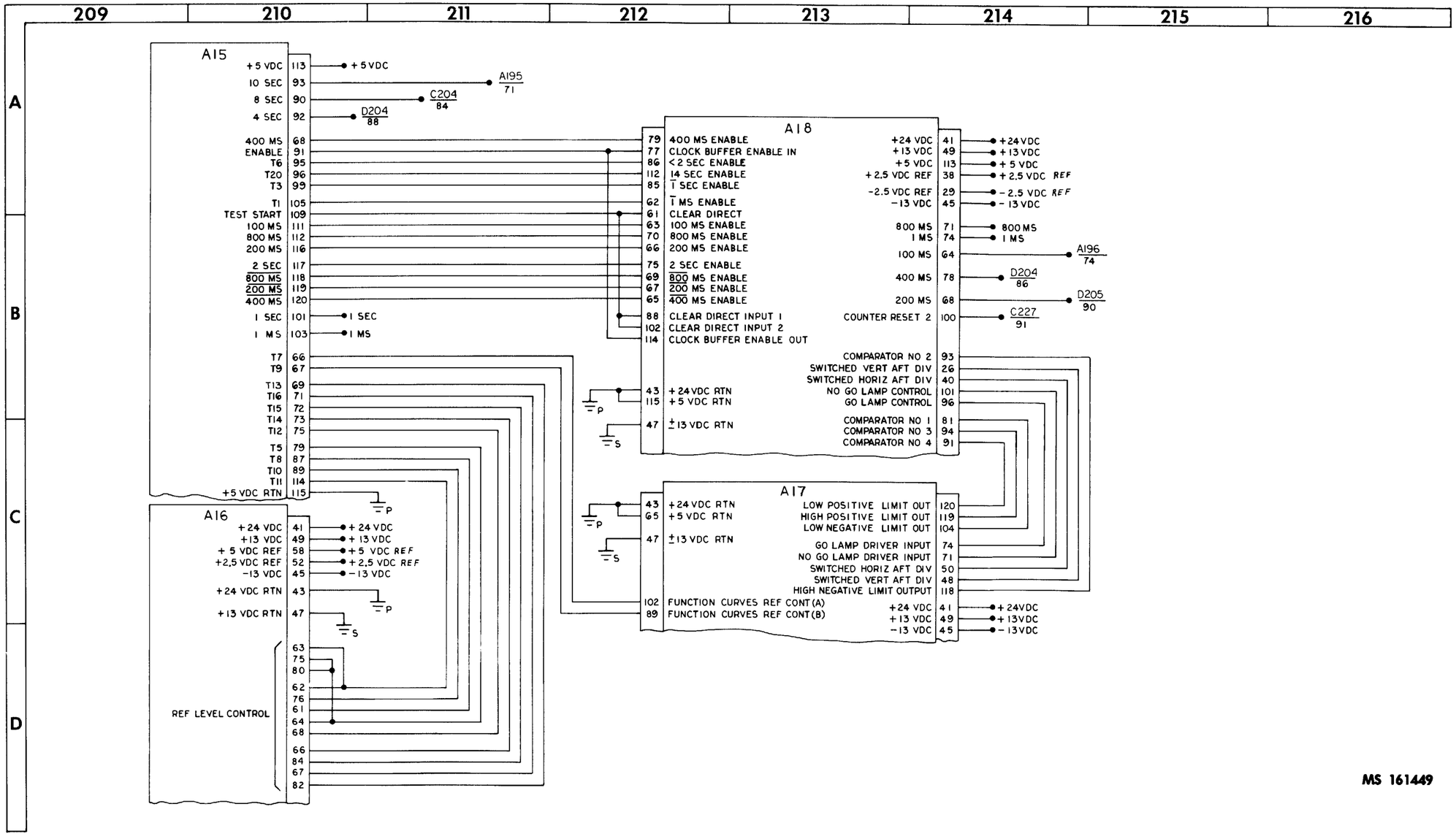


Figure 4-1. DMS-D- schematic diagram (sheet 26 of 30)



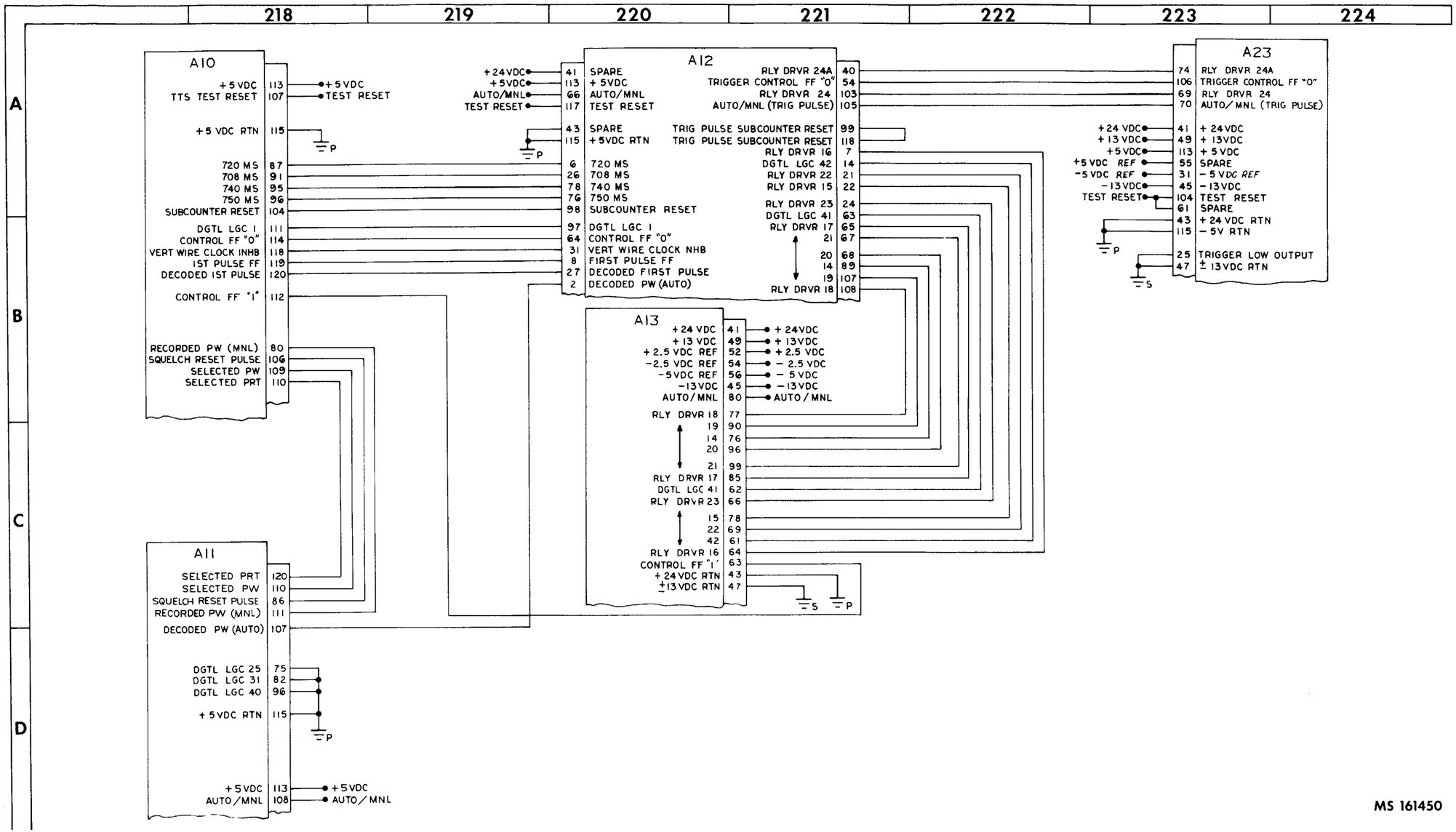
MS 161448

Figure 4-1. DMS-D- schematic diagram (sheet 27 of 30)



MS 161449

Figure 4-1. DMS-D-schematic diagram (sheet 28 of 30)



MS 161450

Figure 4-1. DMS-D - schematic diagram (sheet 29 of 30)

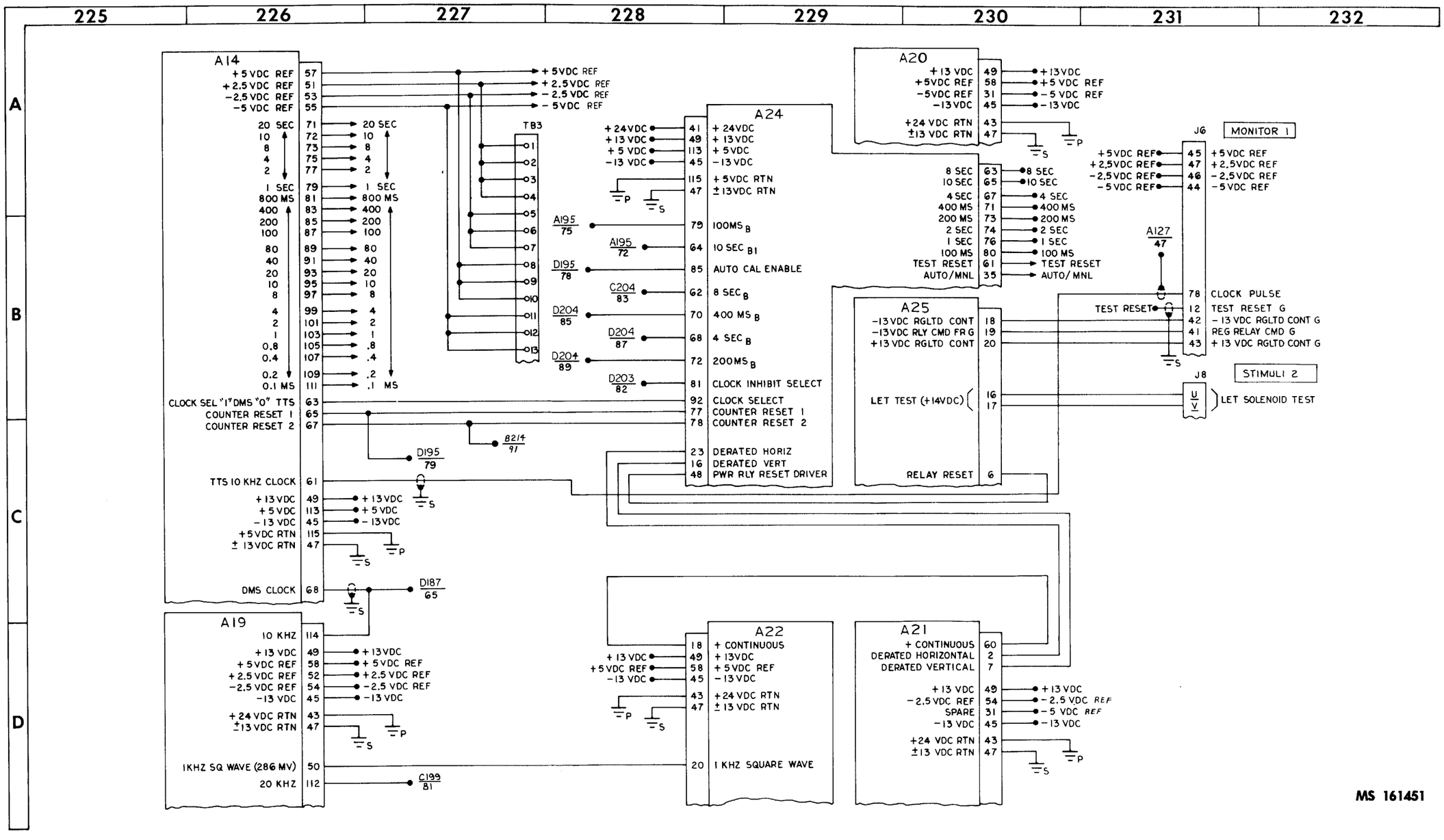
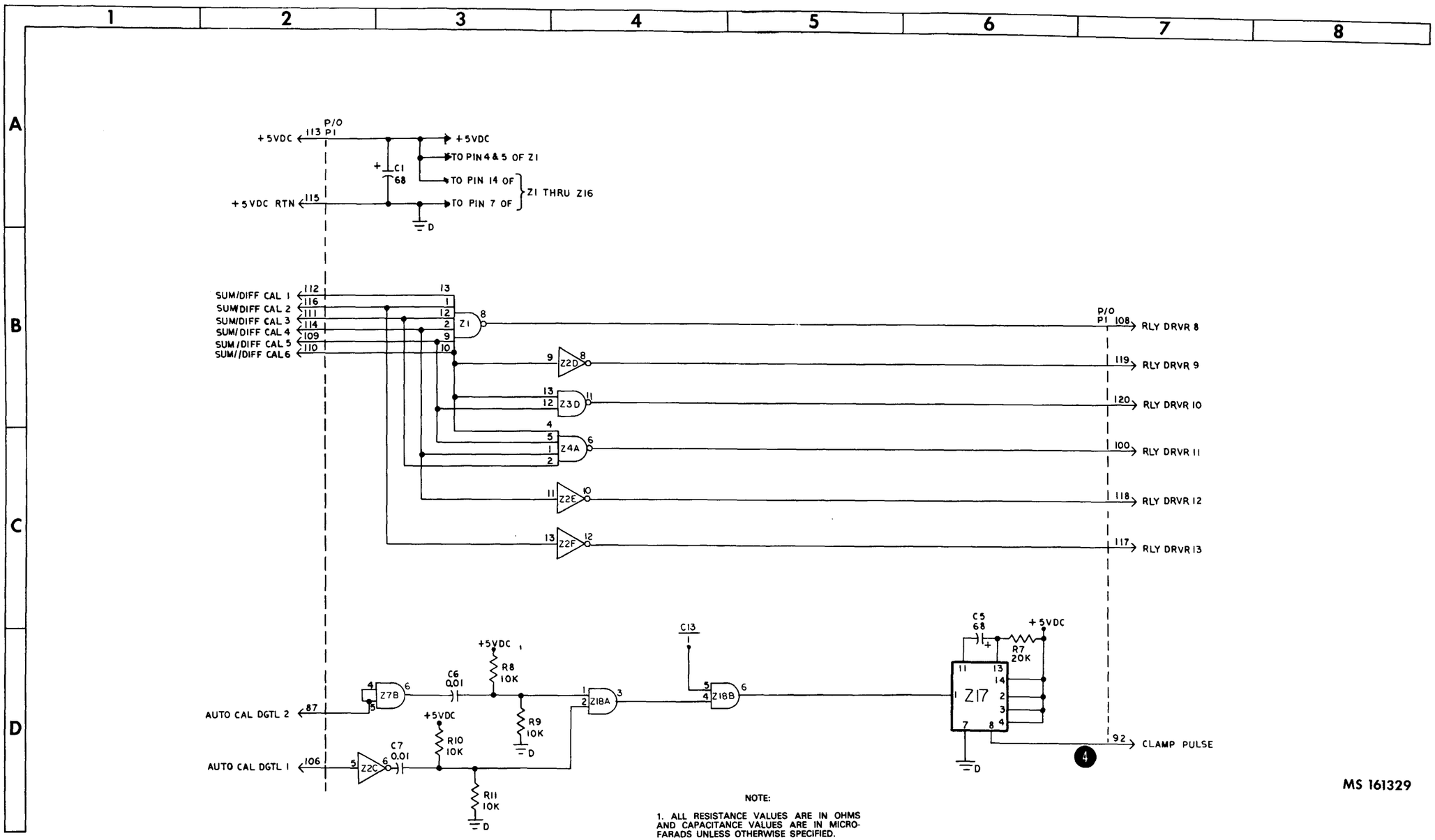


Figure 4-1. DMS-D-schematic diagram (sheet 30 of 30)



MS 161329

Figure 4-2. DMS-D card A1 schematic diagram (sheet 1 of 3)

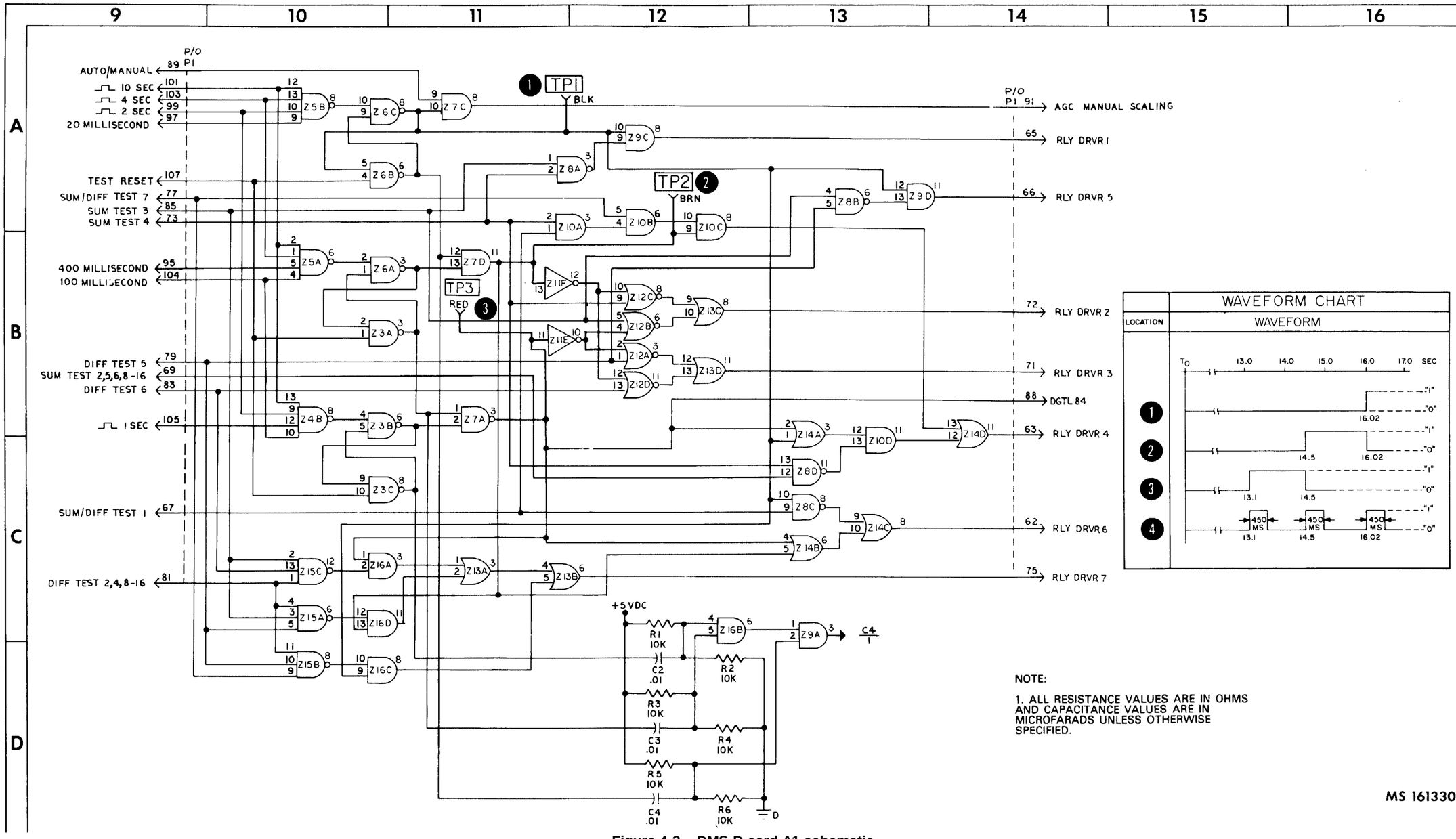
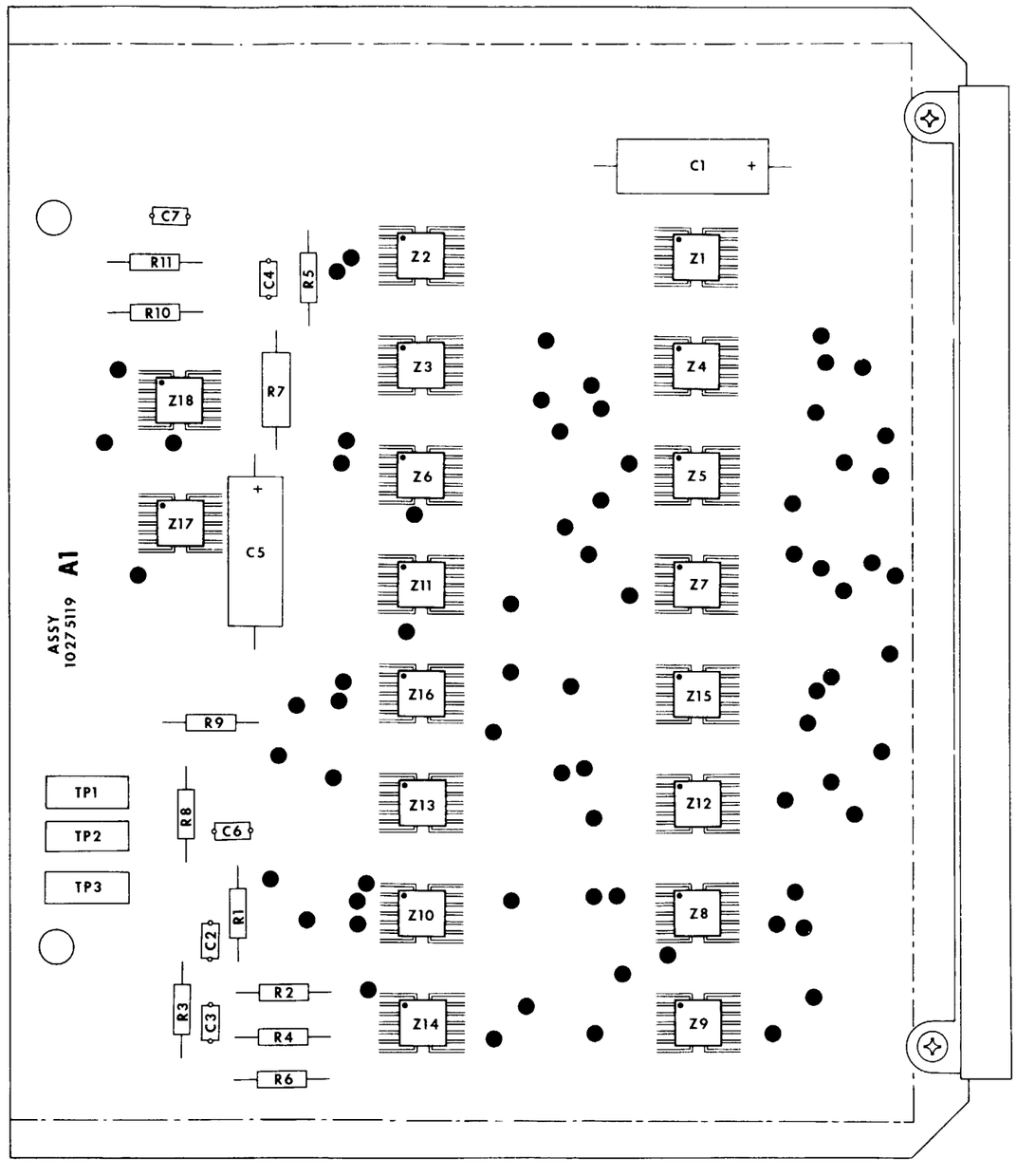
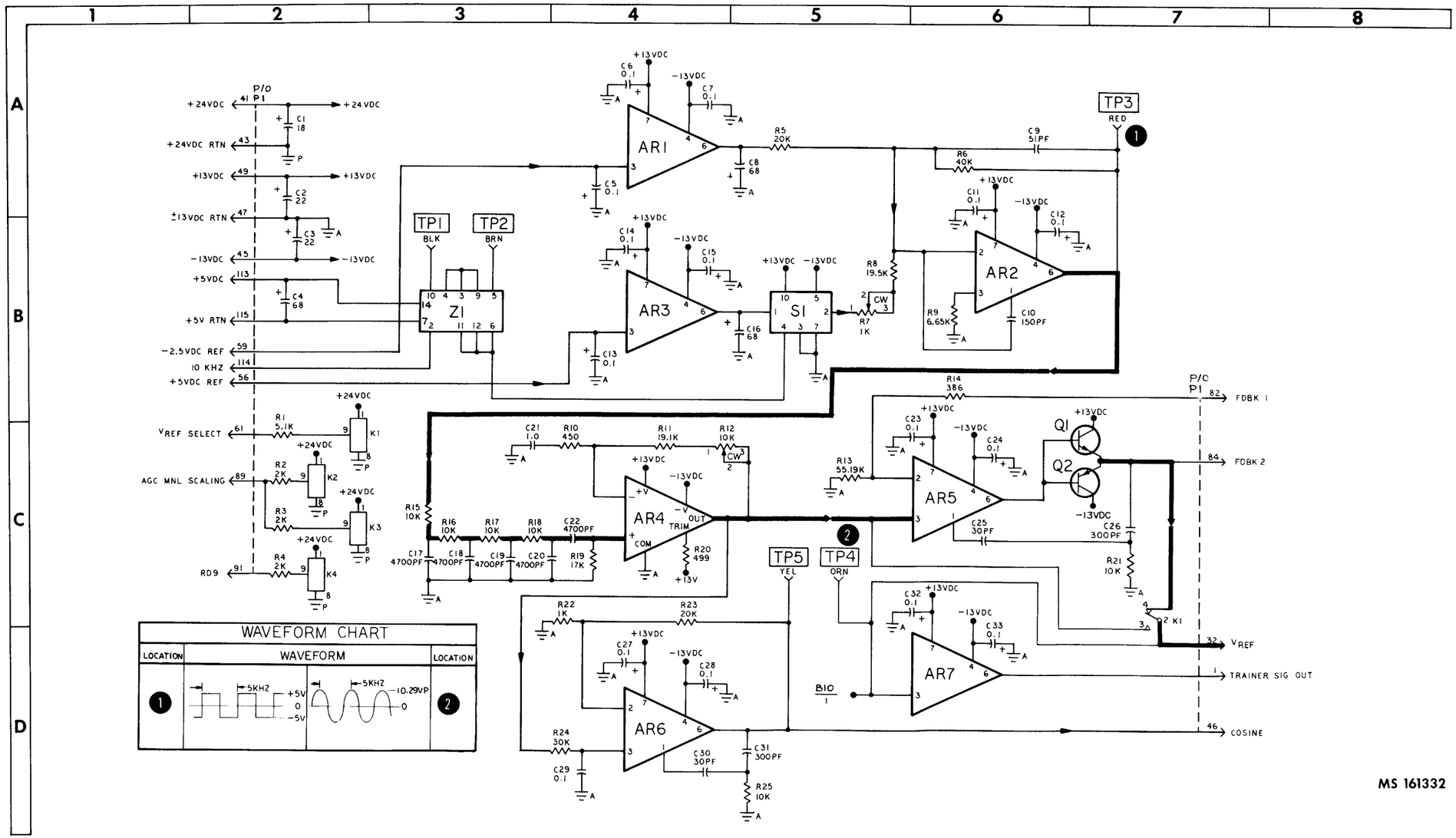


Figure 4-2 . DMS-D card A1 schematic diagram (sheet 2 of 3)



MS 161331

Figure 4-2. DMS-D card A1-schematic diagram (sheet 3 of 3)



MS 161332

Figure 4-3. DMS-D card A2 (10275122)-schematic diagram (sheet 1 of 3)

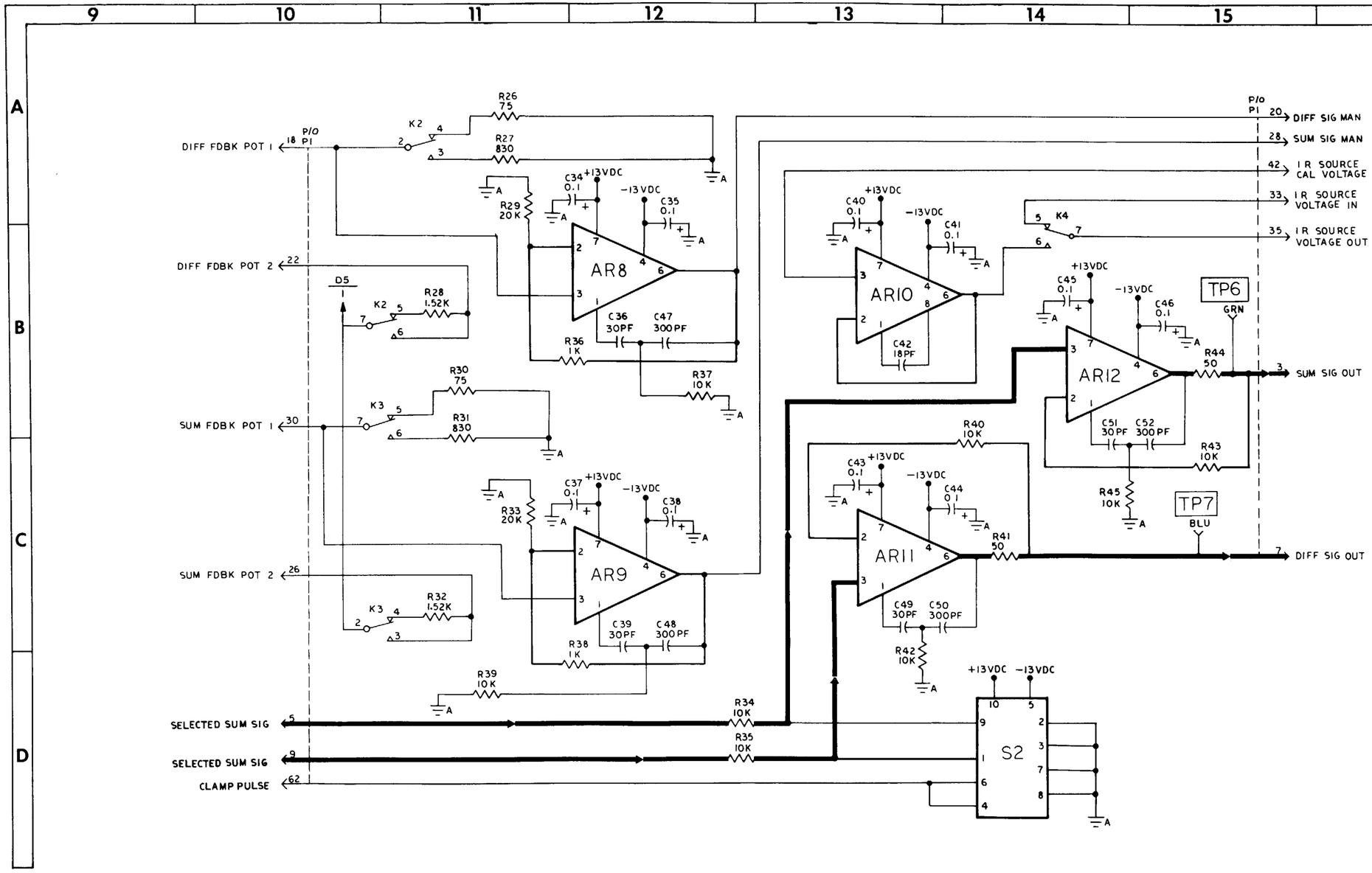
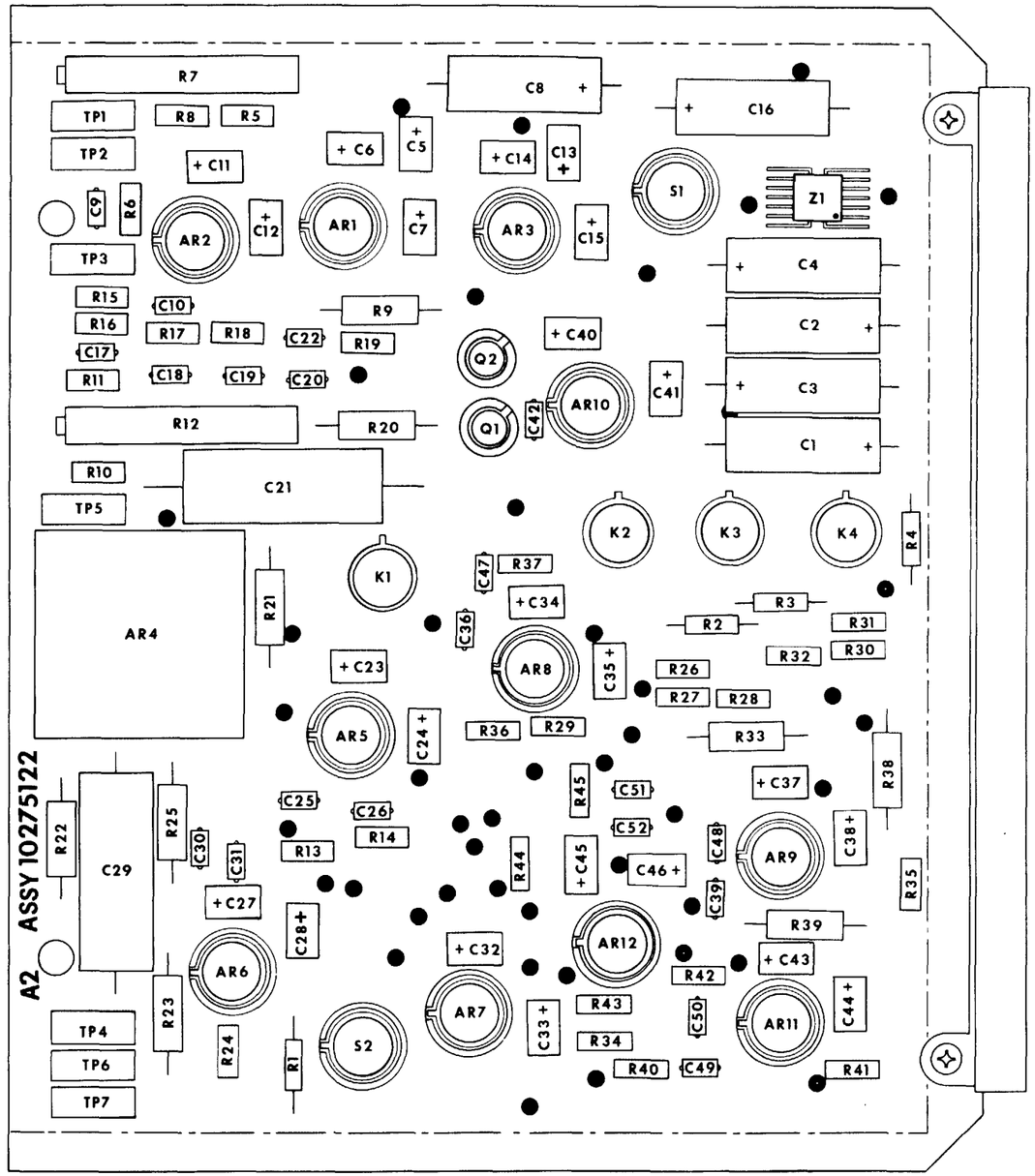
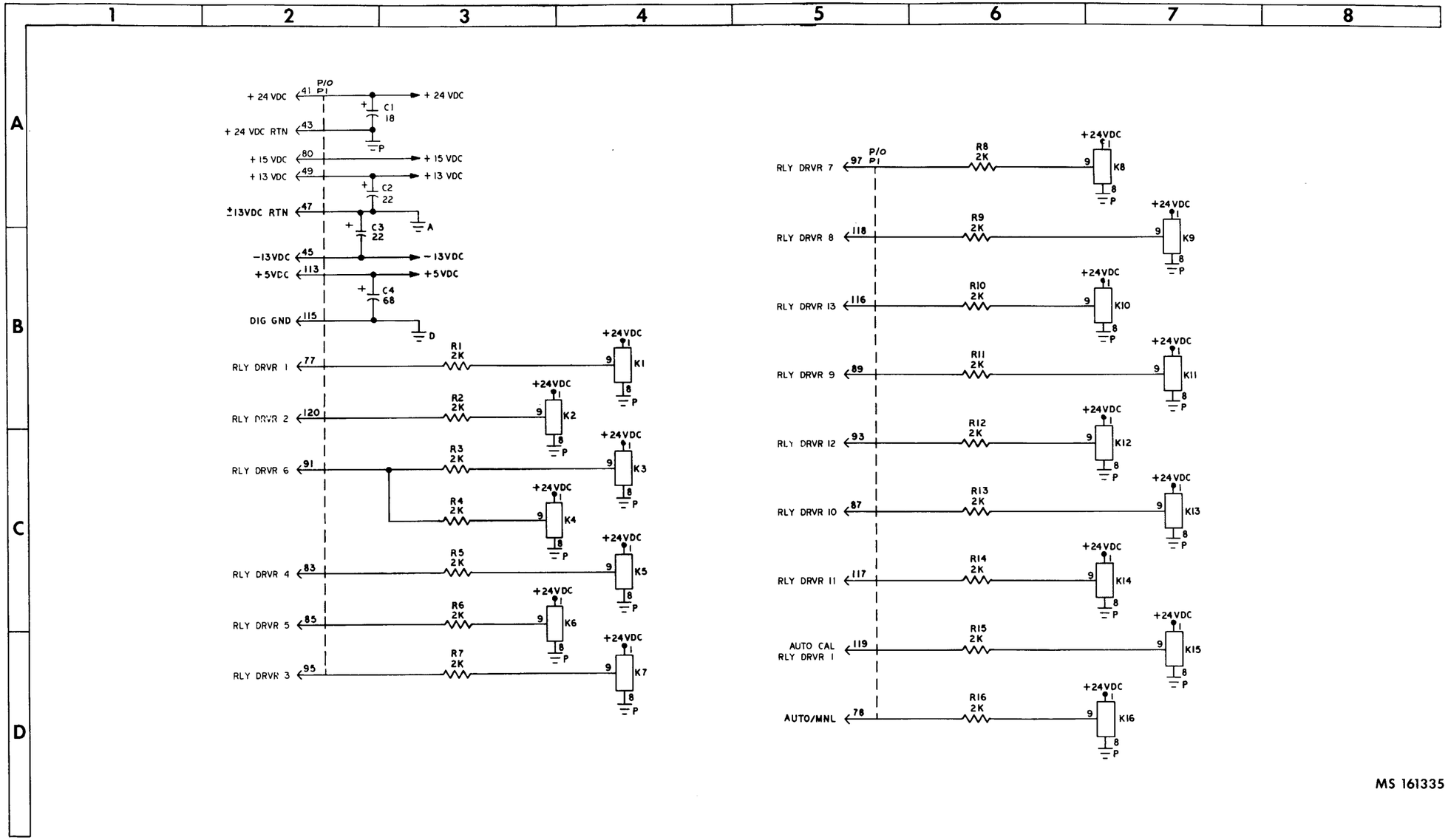


Figure 4-3. DMS-D card A2 (10275122)-schematic diagram (sheet 2 of 3)



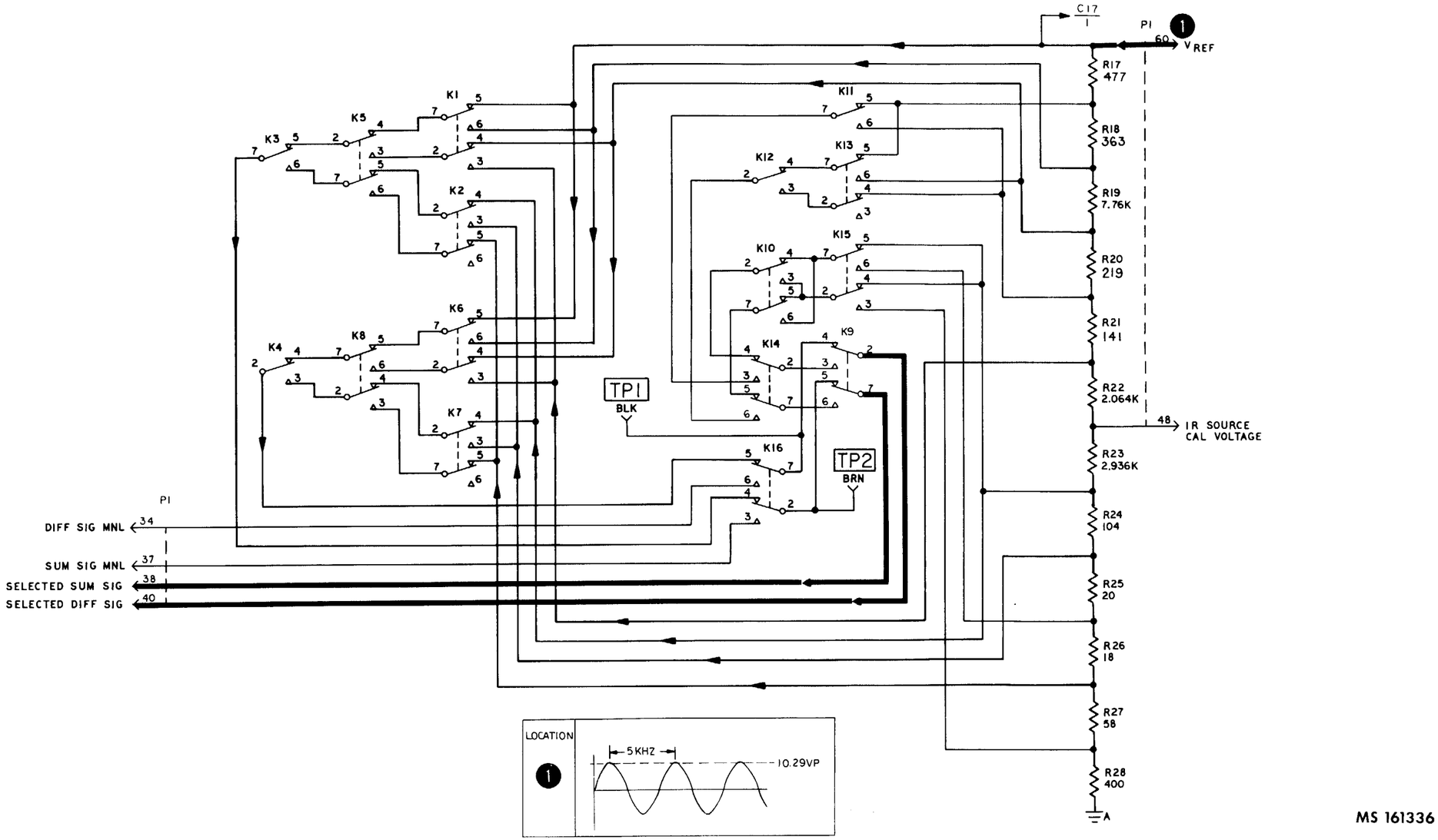
MS 161334

Figure 4-3. DMS-D card A2 - schematic diagram (sheet 3 of 3)



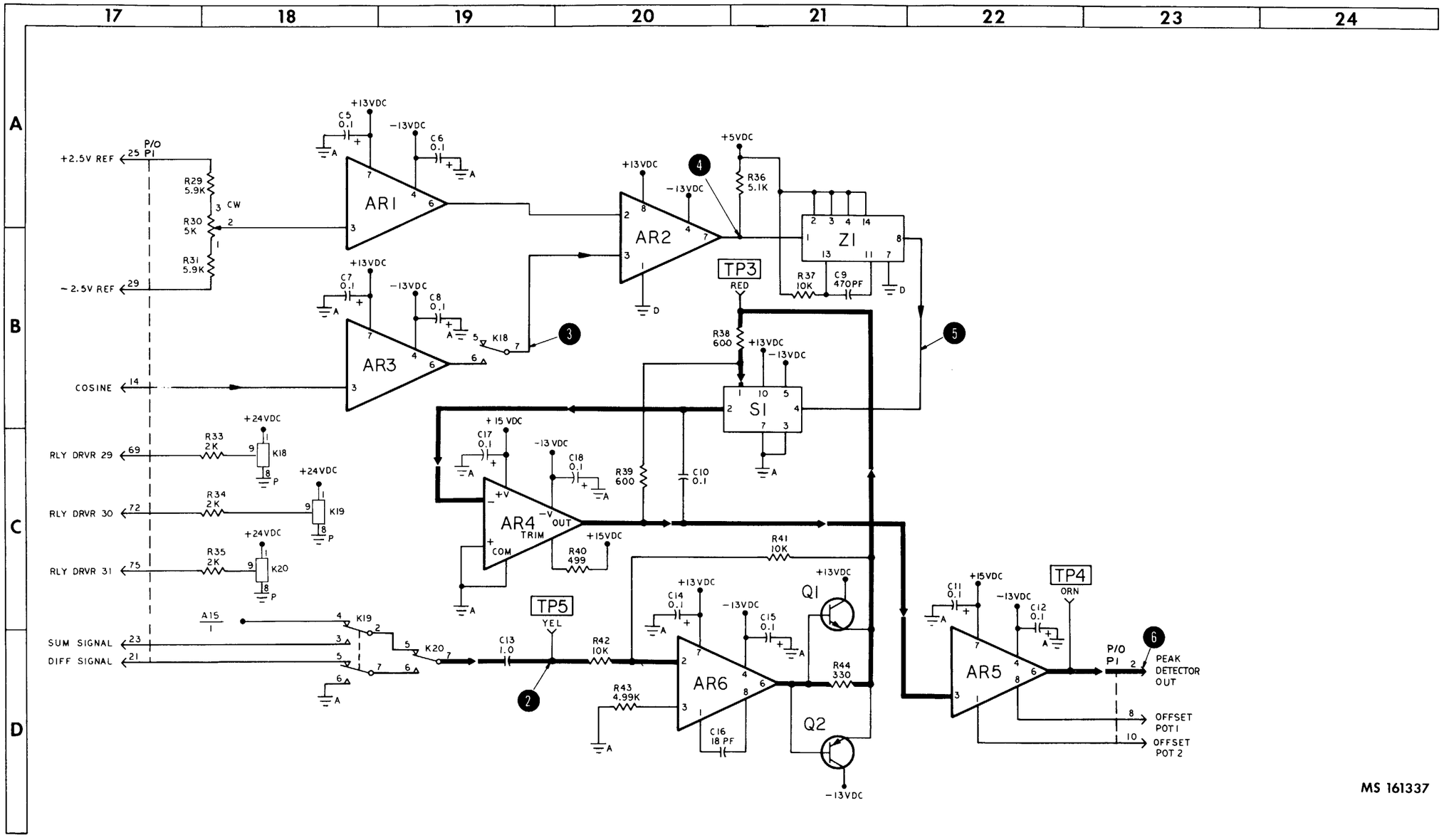
MS 161335

Figure 4-4. DMS-D card A3 (10275143)-schematic diagram (sheet 1 of 4)



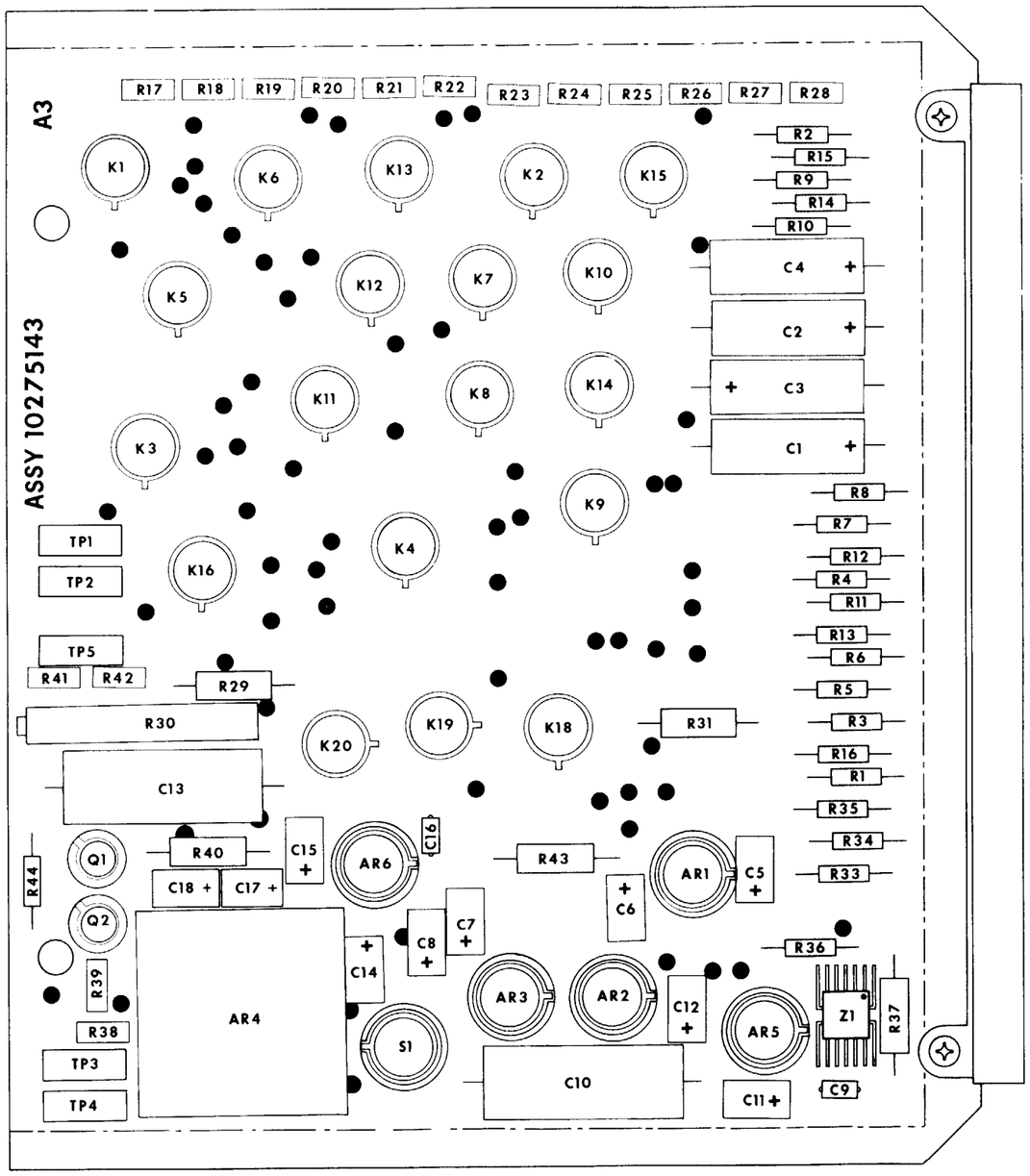
MS 161336

Figure 4-4. DMS-D card A3 (10275143)-schematic diagram (sheet 2 of 4)



MS 161337

Figure 4-4. DMS-D card A3 (10275143)-schematic diagram (sheet 3 of 4)



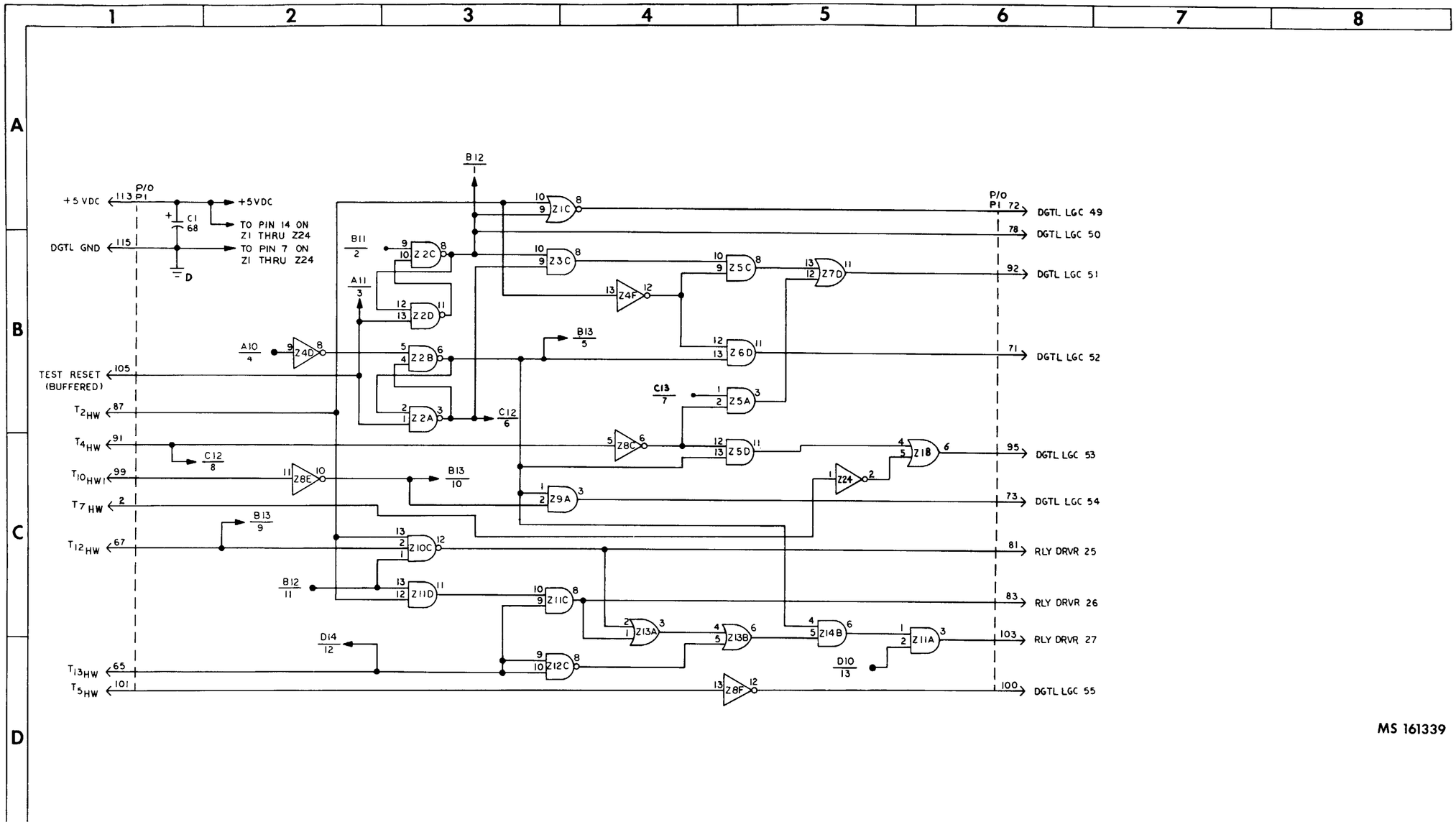
WAVEFORM CHART

LOCATION	WAVEFORM
2	5 KHZ; VP
3 (K18 ENERGIZED)	
4	+4.5 ± 0.5 VDC; LO
5	2 μ SEC; ≥ +2.4 VDC; LO
6	–VP (DC); 0V

LO = ≤ +0.4 VDC

MS 161339

Figure 4-4. DMS-D card A3 - schematic diagram (sheet 4 of 4)



MS 161339

Figure 4-5. DMS-D A card A4 (10275125)-schematic diagram (sheet 1 of 3)

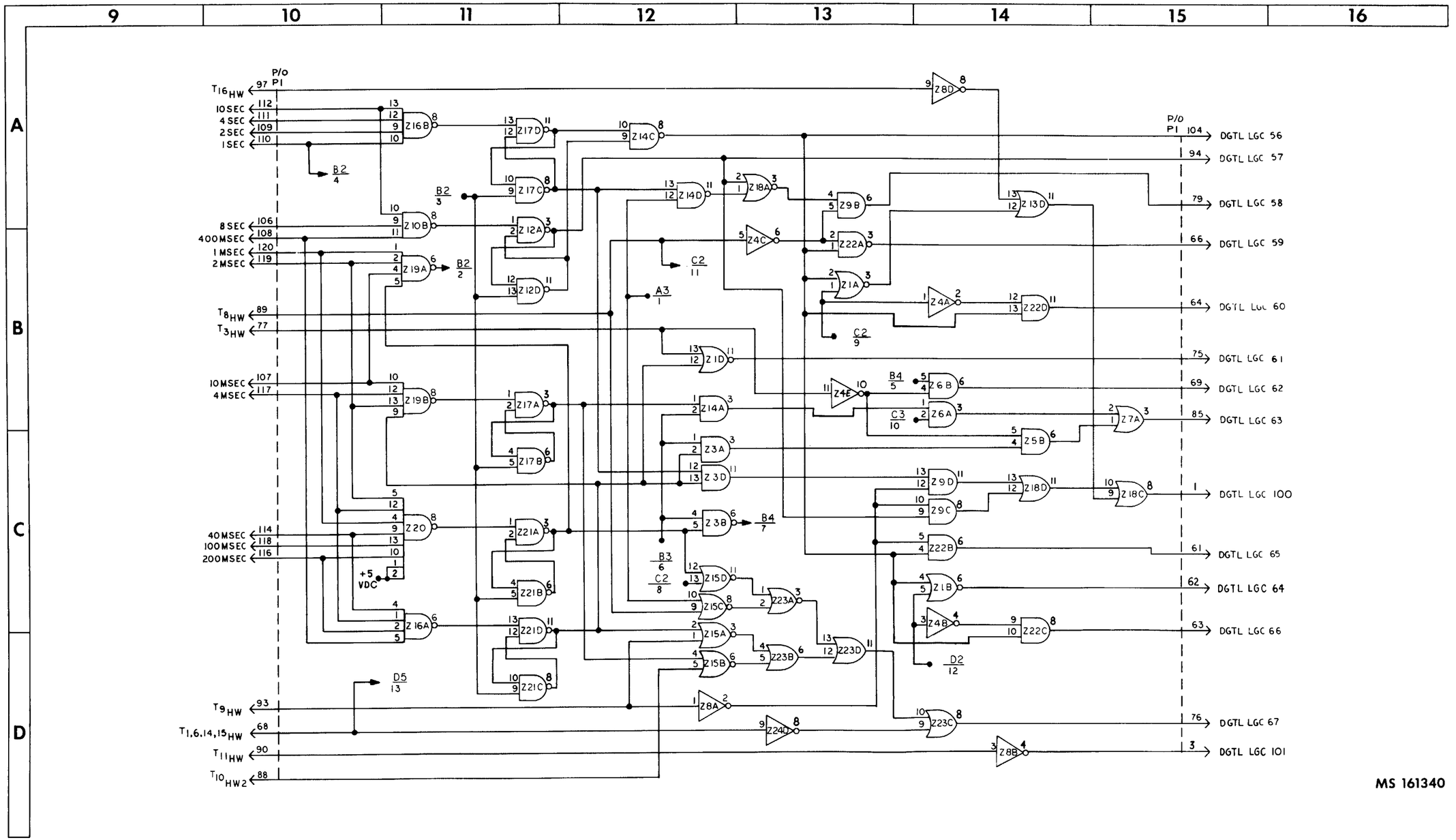
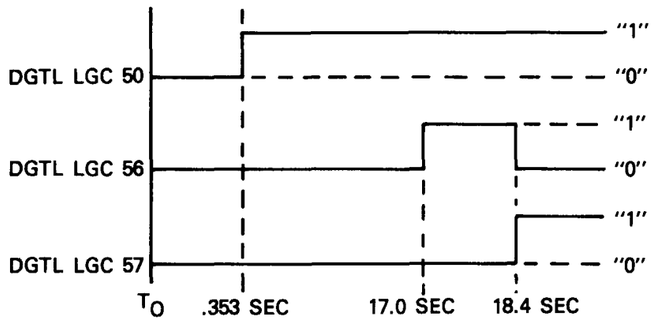


Figure 4-5. DMS-D A card A4 (10275125)-schematic diagram (sheet 2 of 3)



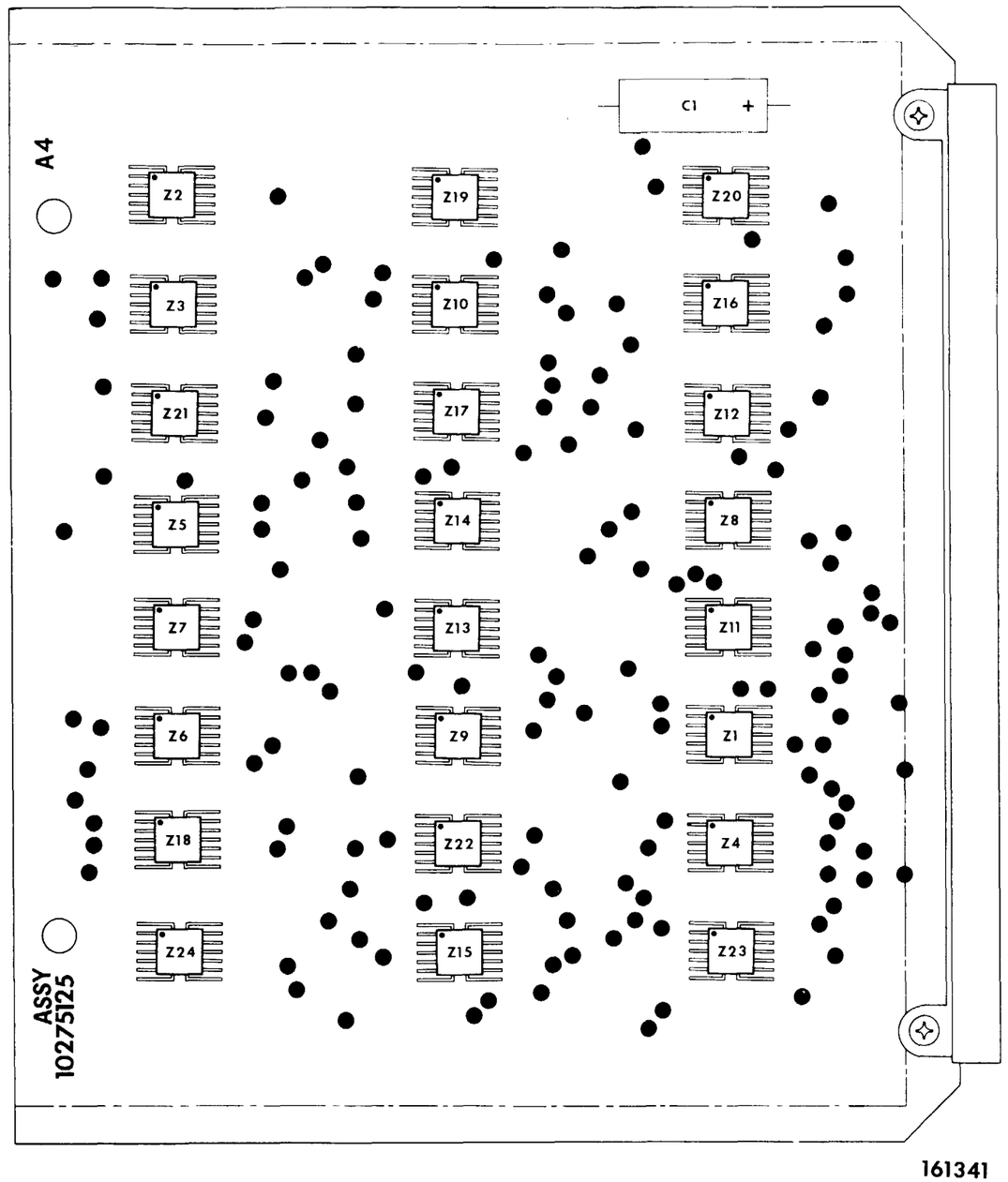


Figure 4-5. DMS-D card A4-schematic diagram (sheet 3 of 3)

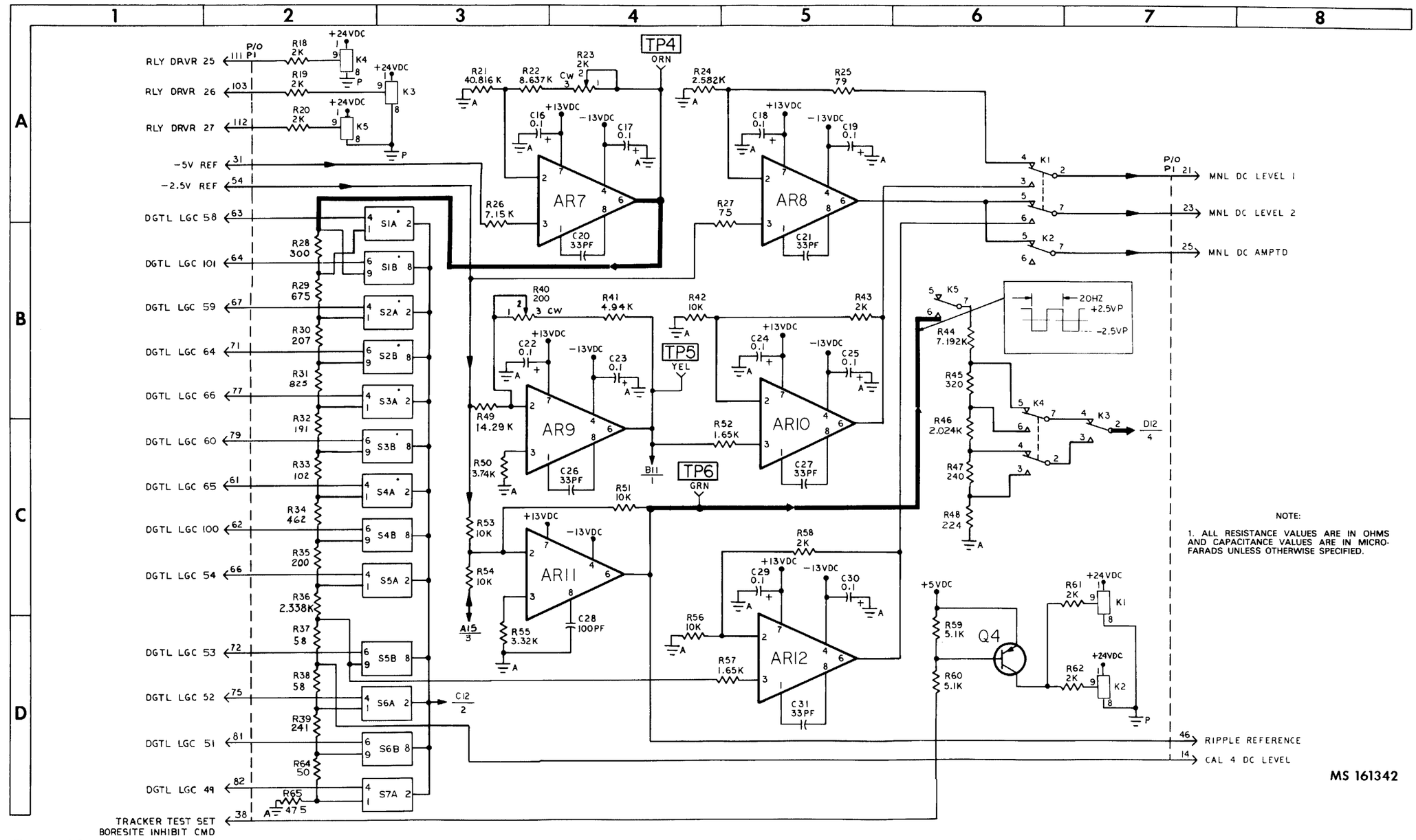


Figure 4-6. DMS-D card A5 schematic diagram (sheet 1 of 3)

Figure 4-6. DMS-D card A5 schematic diagram (sheet 1 of 3)

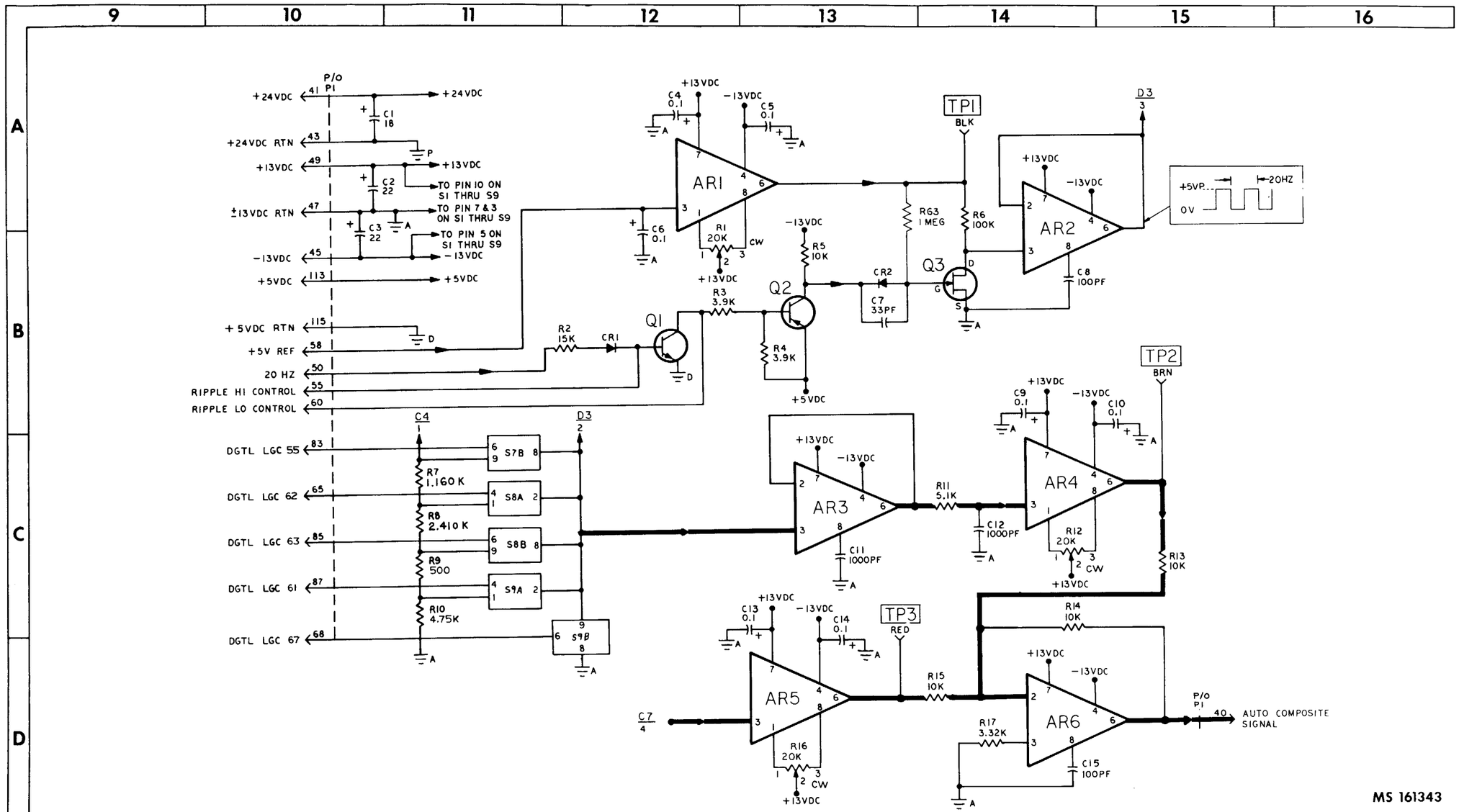


Figure 4-6. DMS-D card A5- schematic diagram (sheet 2 of 3)

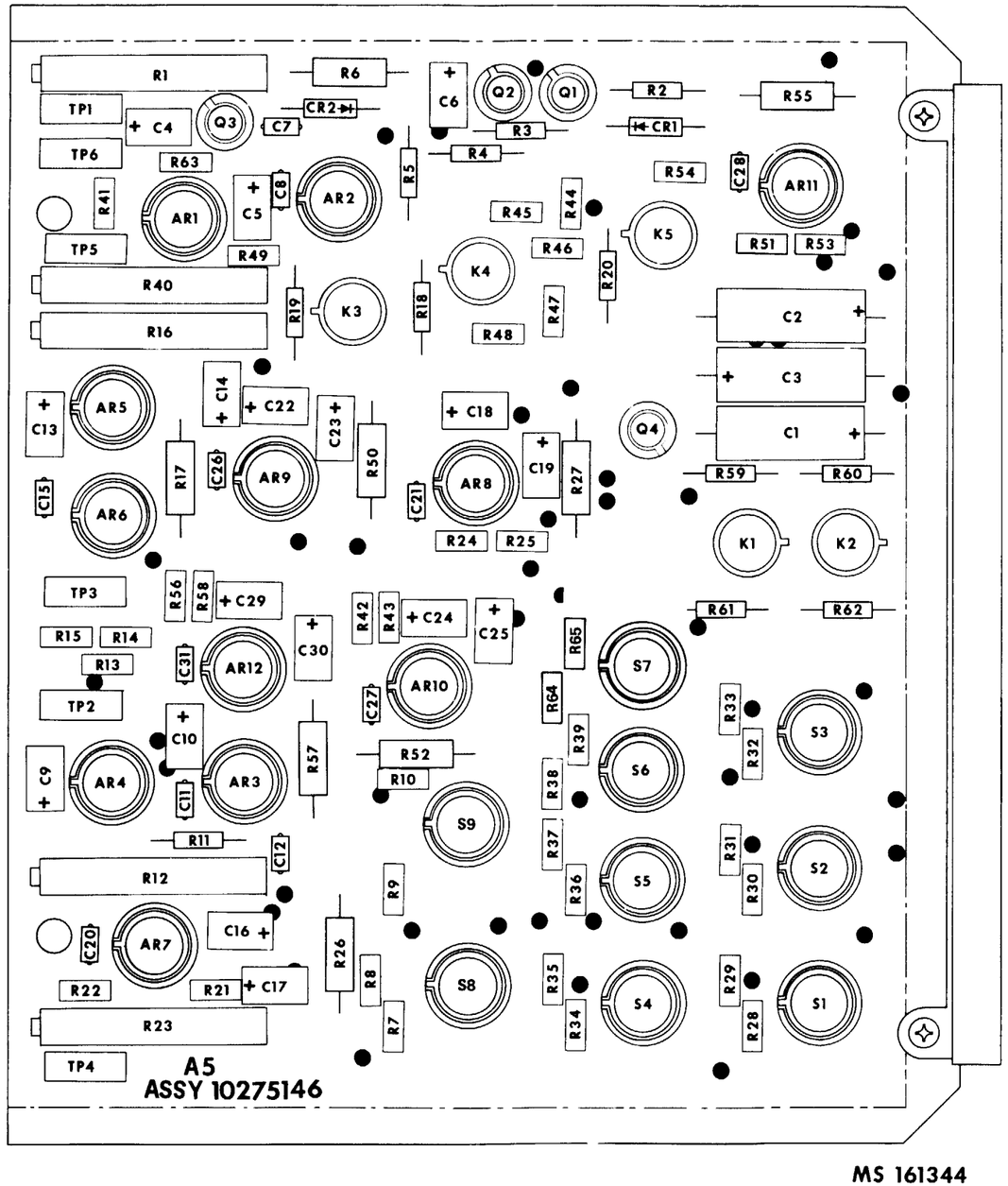


Figure 4-6. DMS-D card A5 schematic diagram (sheet 3 of 3)

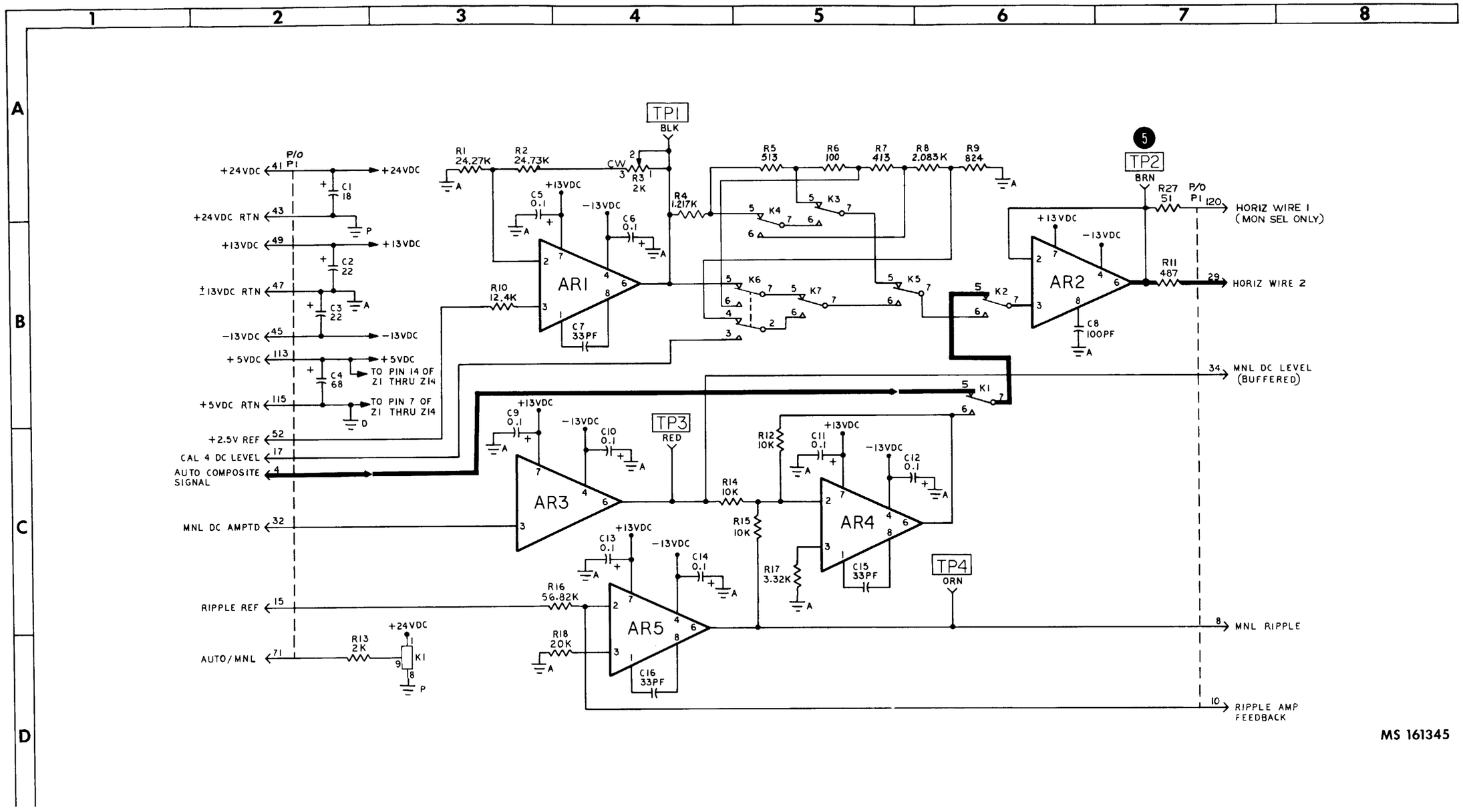
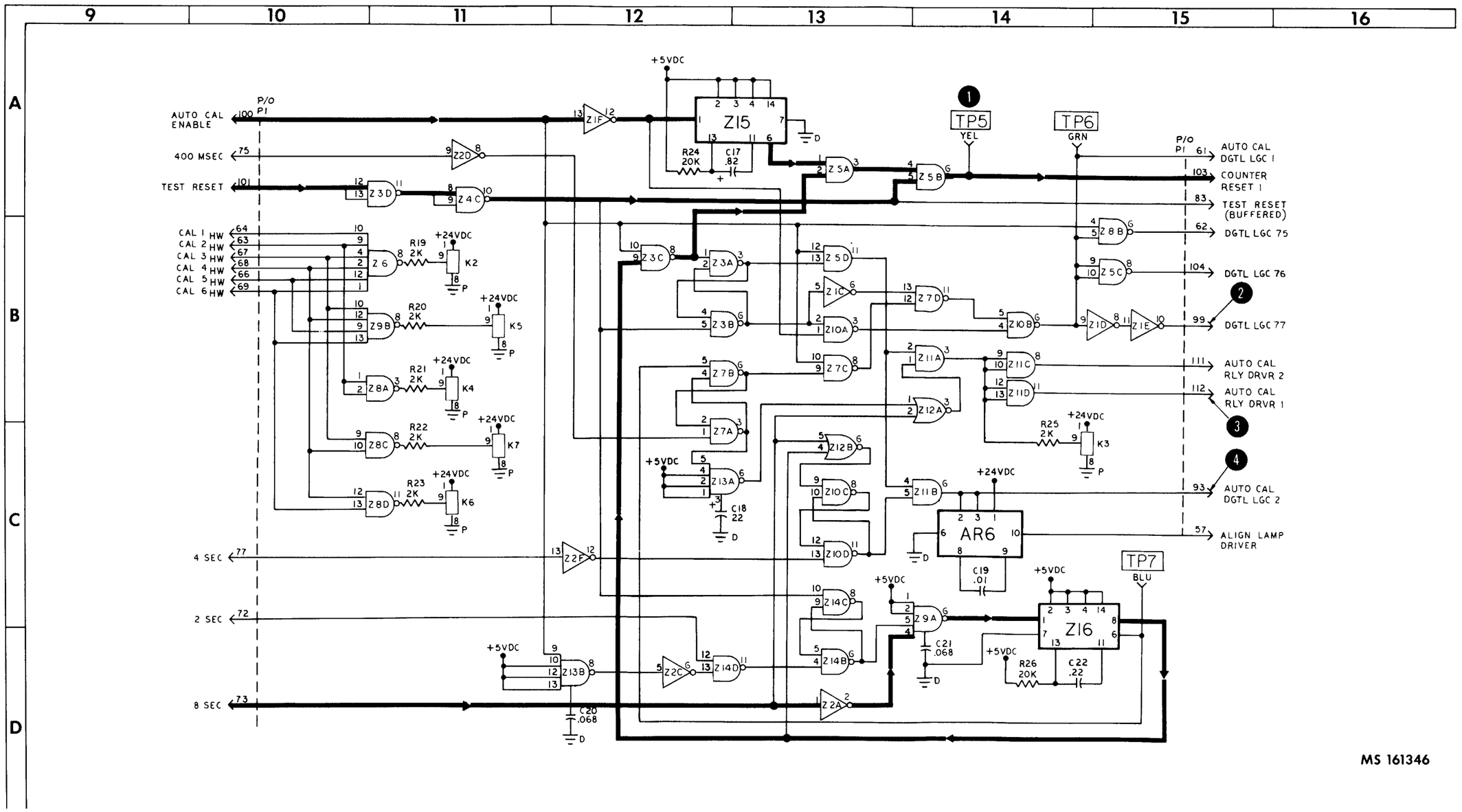


Figure 4-7. DMS-D card A6 - schematic diagram (sheet 1 of 4)



MS 161346

Figure 4-7. DMS-D card A6-schematic diagram (sheet 2 of 4)

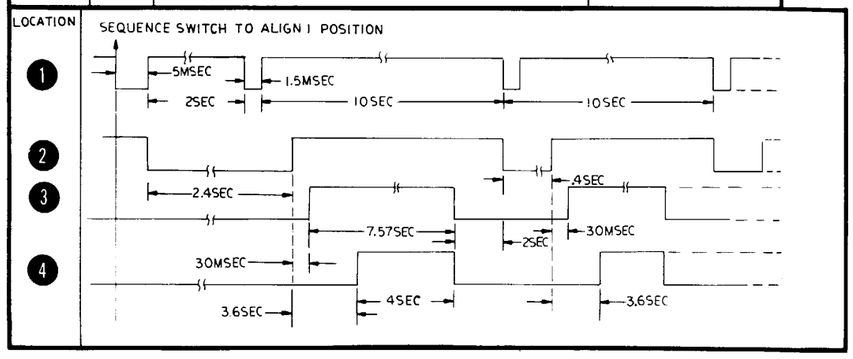
WAVEFORM CHART

SEQ SW POSITION	WAVEFORM LOCATION 5	RIPPLE (20HZ SQ WAVE, INITIATED AT 1 SEC)
1,6, 14,15	0V	0V
2	T0, .353S, +.766V, +.525V, +.475V, 1S, 0V	622 MV PEAK
3	0V, .644S, −.475V, −.525V, −.766V	116 MV PEAK
4	.347S, +.882V, +.525V, 0V	116 MV PEAK
5	0V, -.882	116 MV PEAK
7	+.882, 0V	116 MV PEAK
8	18.4S, 17S, +5.207V, +5.882, 0V	622MV PEAK
9	+3.42V, 0V, +3.882V	116 MV PEAK
10	.656S, +3.22V, 0V, −.525V	116 MV PEAK
11	+6.182V, 0V	116 MV PEAK
12	+3.42V, 0V, +3.984V	56 MV PEAK
13	+5.00V, 0V, +4.175V	702MV PEAK
16	+3.42V, 0V	116 MV PEAK

HI = ≥ +2.4 VDC LO = ≤ +0.4VDC

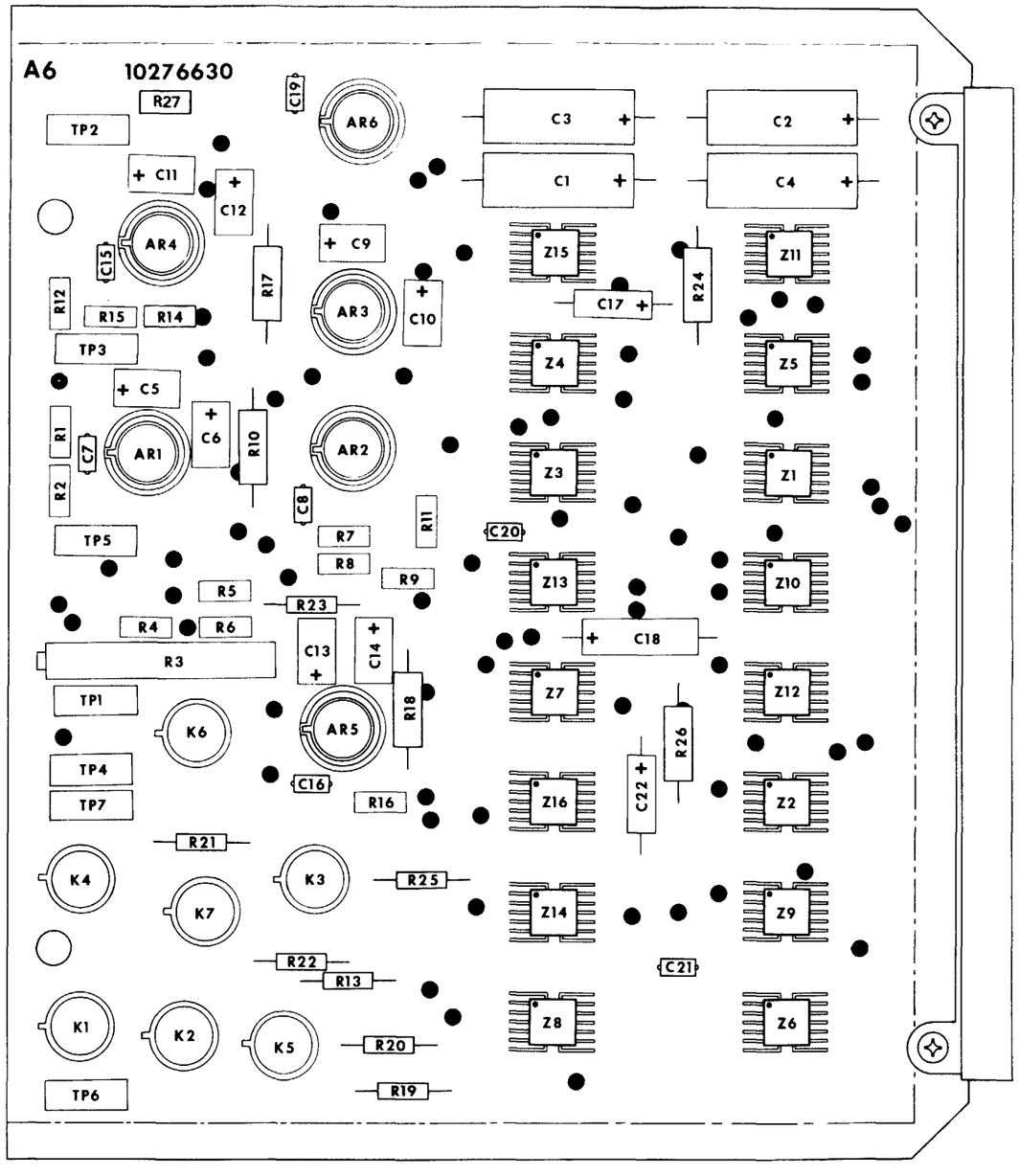
WAVEFORM CHART

SEQ SW POSITION	WAVEFORM LOCATION 5	REMARKS
MNL	[TTS BORESIGHT MODE (INTERNAL TEST SW, POSITION 4)] VARIABLE −1.058V TO +1.058 VDC TTS MISSILE COMMAND MODE: VARIABLE +2.576V TO +7.418 VDC	RIPPLE (20HZ SQ WAVE) VARIABLE 0V TO 871 MV PEAK
ALIGN 1	T0, 9.6S, .4S, 2.4S, 3.6S, ALIGN LT, HI, LO, 2S, 7.57S, 30MS, 2.43S, +3.933V, +3.42V, 0V	J7-42 CONTROLLED AS SHOWN. T0 IS SEQUENCE SW TRANSFER FROM MNL TO ALIGN 1 OR ALIGN 2
ALIGN 2	+3.42V, +2.907V, 0V	
ALIGN 3	+824 MVDC (NO RIPPLE)	
ALIGN 4	−824 MVDC (NO RIPPLE)	
ALIGN 5	+5.15 VDC (NO RIPPLE)	
ALIGN 6	+3.32 VDC (NO RIPPLE)	



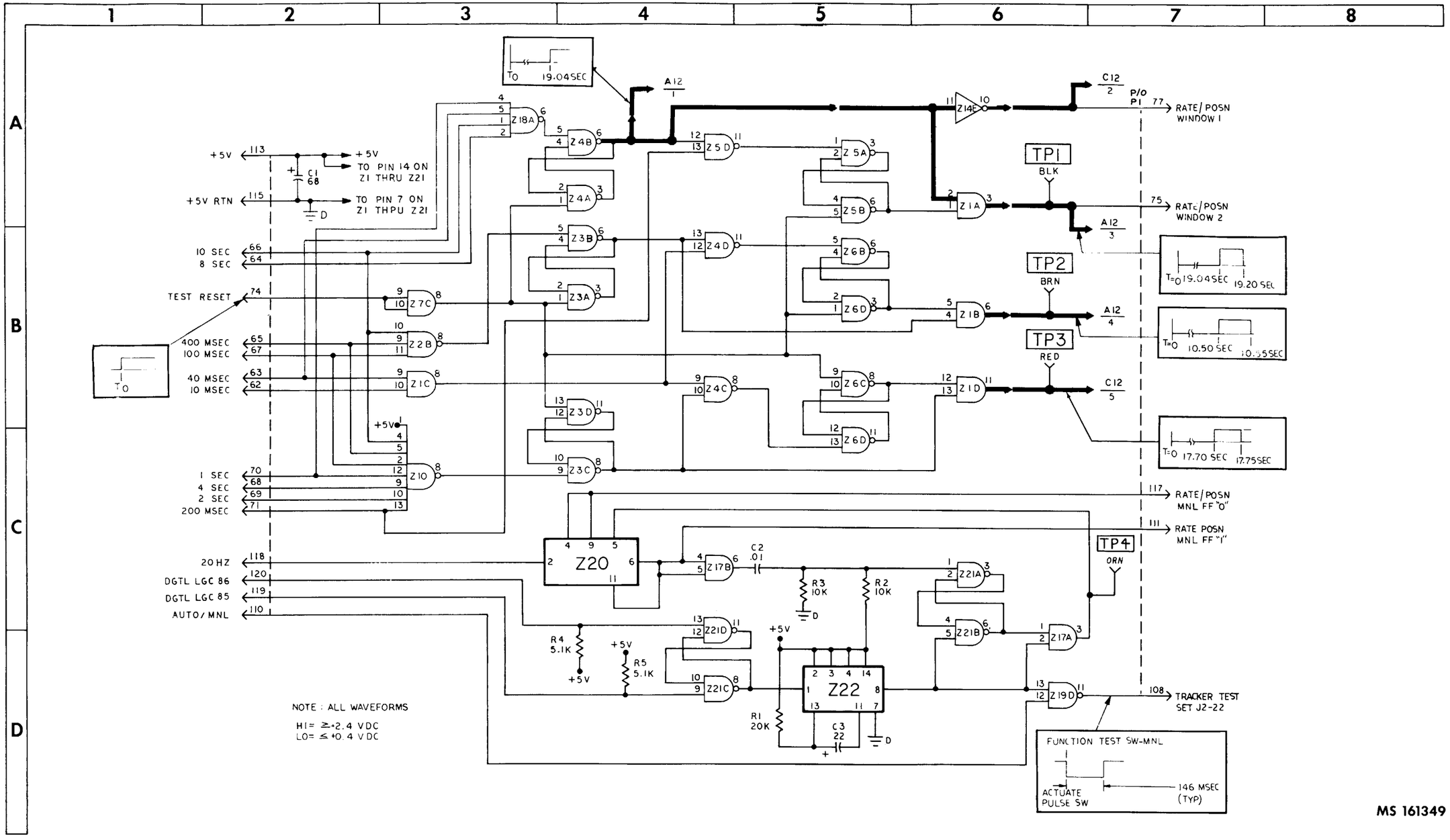
MS161347

Figure 4-7. DMS-D card A6- schematic diagram (sheet 3 of 4)



MS161348

Figure 4-7. DMS-D card A6-schematic diagram (sheet 4 of 4)



MS 161349

Figure 4-8. DMS-D card A7 (10275134)-schematic diagram (sheet 1 of 3)

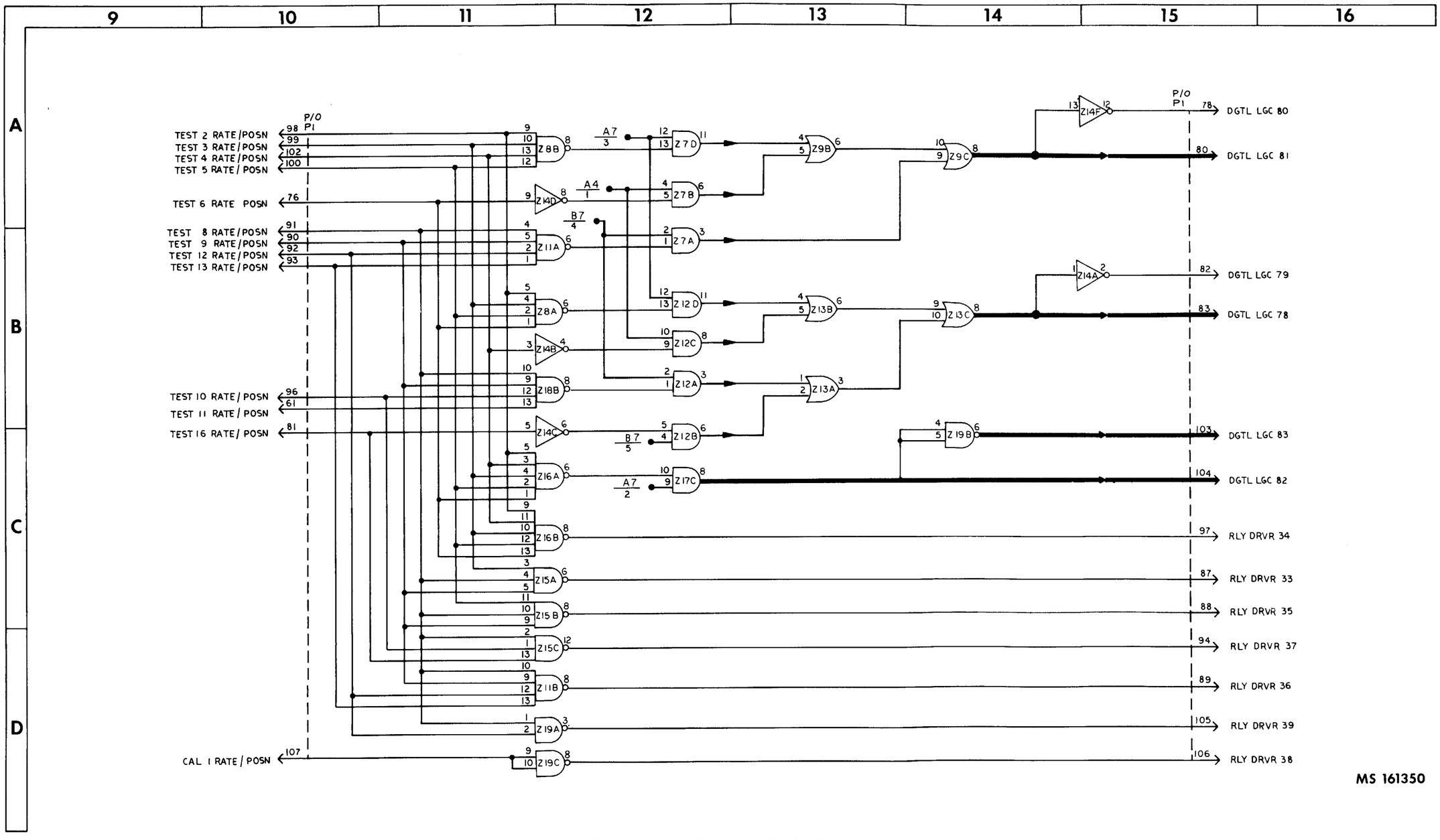


Figure 4-8. DMS-D card A7 (10275134)-schematic diagram (sheet 2 of 3)

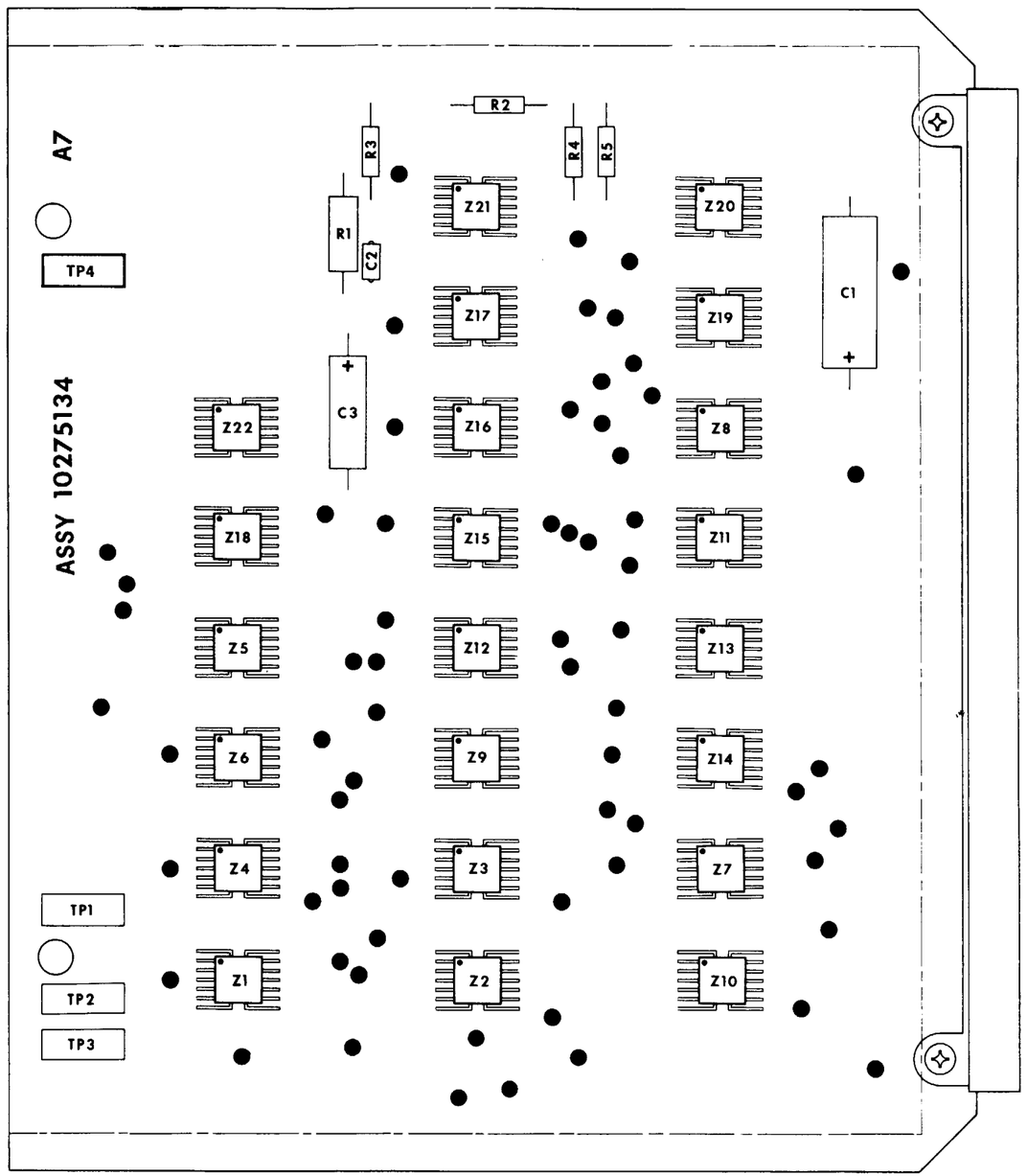


Figure 4-8. DMS-D card A7 (10275134)-schematic diagram (sheet 3 of 3)

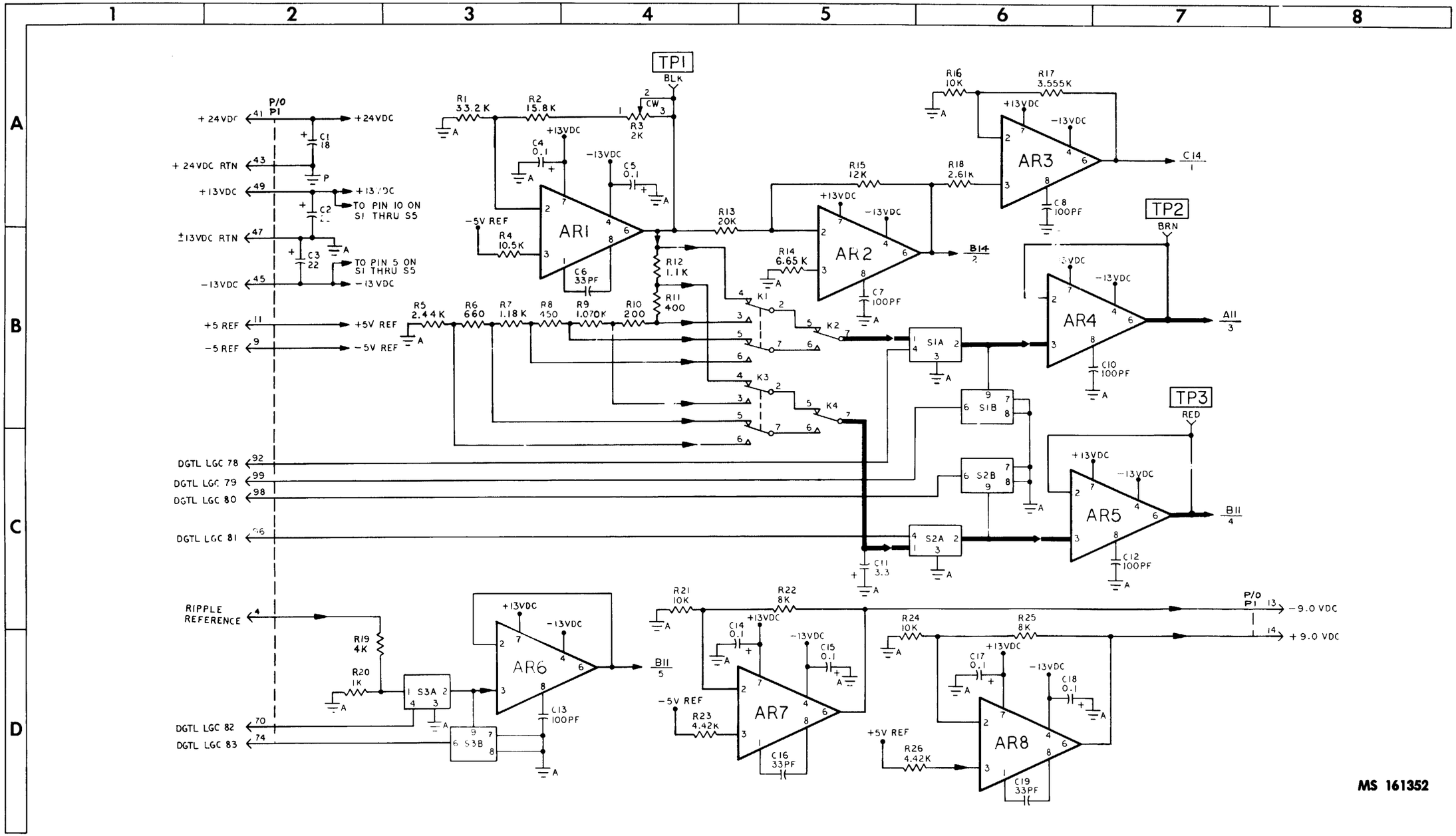


Figure 4-9. DMS-D card A8 schematic diagram (sheet 1 of 4)

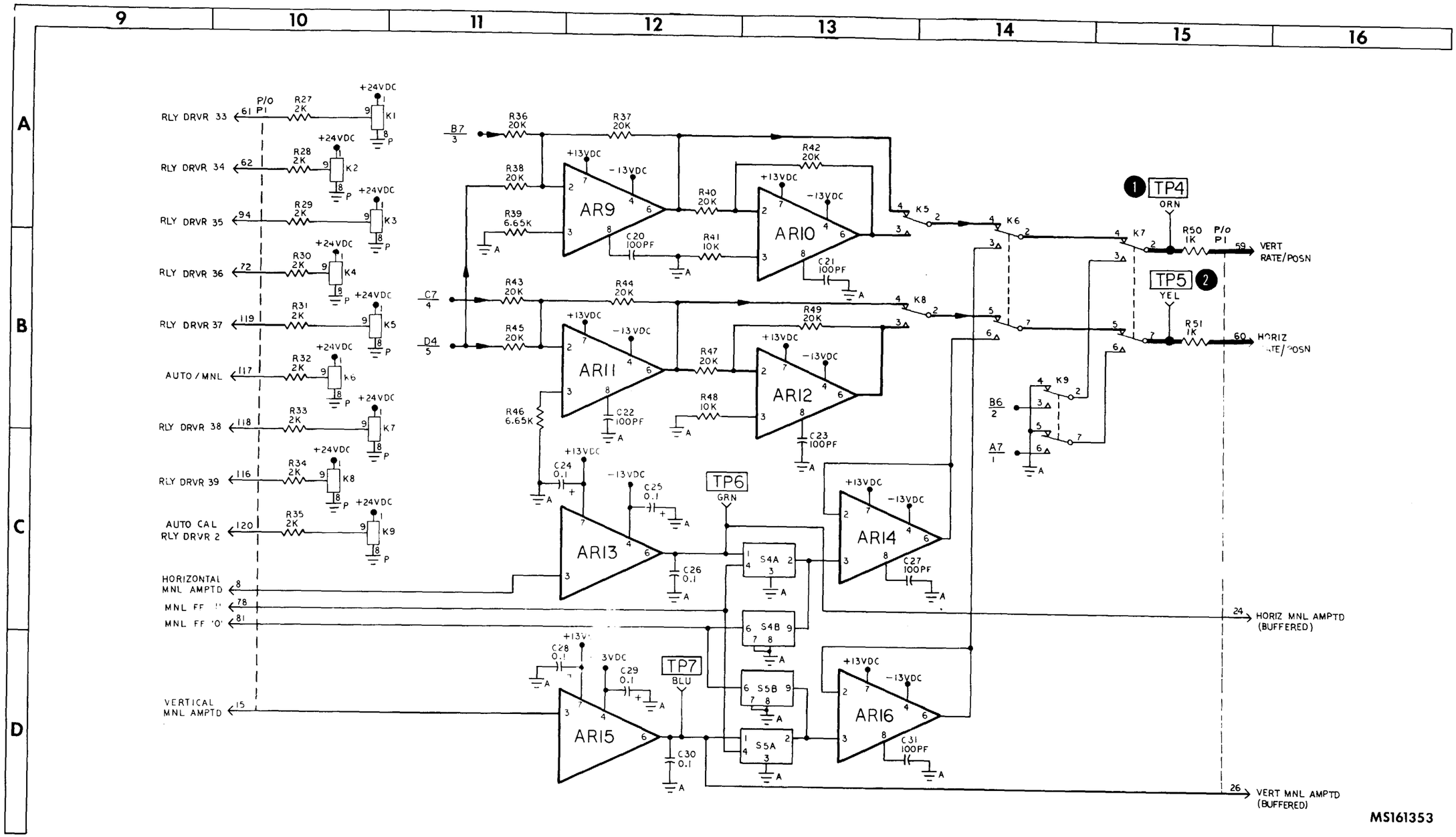


Figure 4-9. DMS-D card A8-schematic diagram (sheet 2 of 4)

WAVEFORM CHART (VERTICAL)

SEQUENCE SW POSITION	WAVEFORM LOCATION ❶
1,7, 12 THRU 15	0 V
2,5,6	TO, 19.04S, 19.20S; 0.5 V, 0V; 20 HZ RIPPLE; +4.73 V
3	0.5 V, 0 V; 20 HZ RIPPLE; +4.28 V
4	0.5V, 0 V; 20 HZ RIPPLE; +4.73 V
8	10.50 S, 10.55 S; 0 V; -6.00 V
9	+6.00 V; 0 V
10	0 V; -7.5 V
11	+7.5 V; 0 V
16	17.70 S, 17.75 S; 0 V; -7.5 V
MNL	TO, 146 ± 44 MS; HI, LO; 0 TO 50 MS; 50 MS; +9 V; -9 V J7–22 CONTROLLED AS SHOWN. 50 MS, VARIABLE AMP PULSE INITIATED BY PULSE SWITCH (TO)
ALIGN 1	TO, 2.4 S, 3.6 S, 9.6 S, ALIGN LT, 3.6 S, ALIGN LT; HI, LO; 2S, 0.4 S; 30 MS, 30 MS; +4.5 V, 0 V; 7.57 S, 2.43 S J7–22 CONTROLLED AS SHOWN. TO IS SEQUENCE SW TRANSFER FR MNL TO ALIGN 1

HI = ≥ +2.4 VDC

WAVEFORM CHART (HORIZONTAL)

SEQUENCE SW POSITION	WAVEFORM LOCATION ❷
1,7,10,11, 14 THRU 16	0 V
2,3,4	TO, 19.04 S, 19.20 S; 0.5 V, 0 V; 20 HZ RIPPLE; +6.4 V
5	0.5 V, 0 V; 20 HZ RIPPLE; +5.8 V
6	0.5 V, 0 V; 20 HZ RIPPLE; +6.4 V
8	10.50 S, 10.55 S; 0 V; -2.44 V
9	+2.44 V; 0 V
12	0 V; -3.1 V
13	+3.1 V; 0 V
MNL	TO, 146 ± 44 MS; HI, LO; 0 TO 50 MS; 50 MS; +9 V; -9 V J7–22 CONTROLLED AS SHOWN. 50 MS, VARIABLE AMPTD PULSE INITIATED BY PULSE SWITCH (TO)
ALIGN 1	TO, 2.4 S, 3.6 S, 9.6 S, ALIGN LT, 3.6 S, ALIGN LT; HI, LO; 2 S, 0.4 S; 30 MS, 30 MS; +6.1 V, 0 V; 7.57 S, 2.43 S J7–22 CONTROLLED AS SHOWN. TO IS SEQUENCE SW TRANSFER FR MNL TO ALIGN 1

MS 161354

Figure 4-9. DMS-D card A8- schematic diagram (sheet 3 of 4)

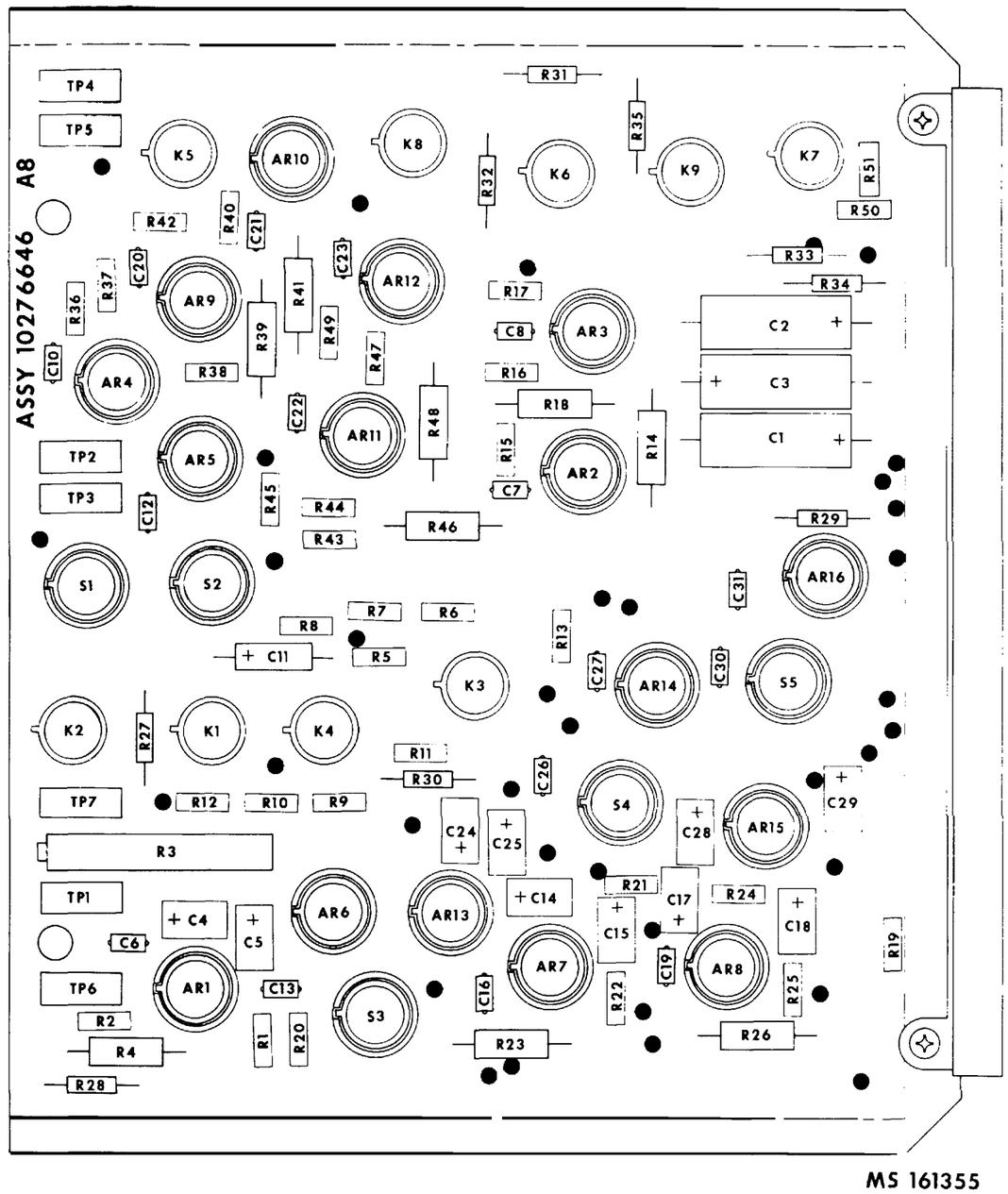
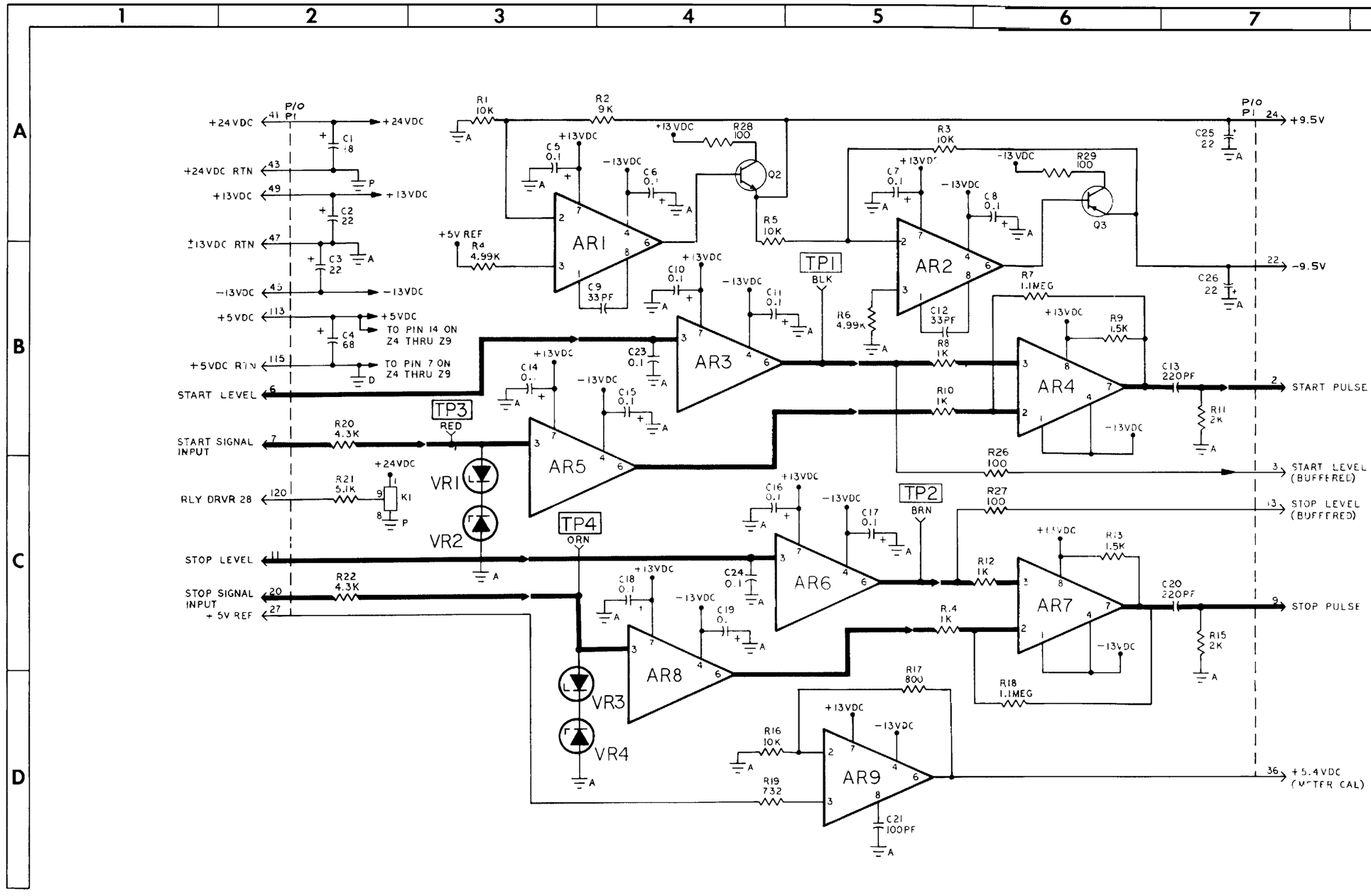


Figure 4-9. DMS-D card A8 schematic diagram (sheet 4 of 4)



MS 161356

Figure 4-10. DMS-D card A8 (10275402) - schematic diagram (sheet 1 of 3)

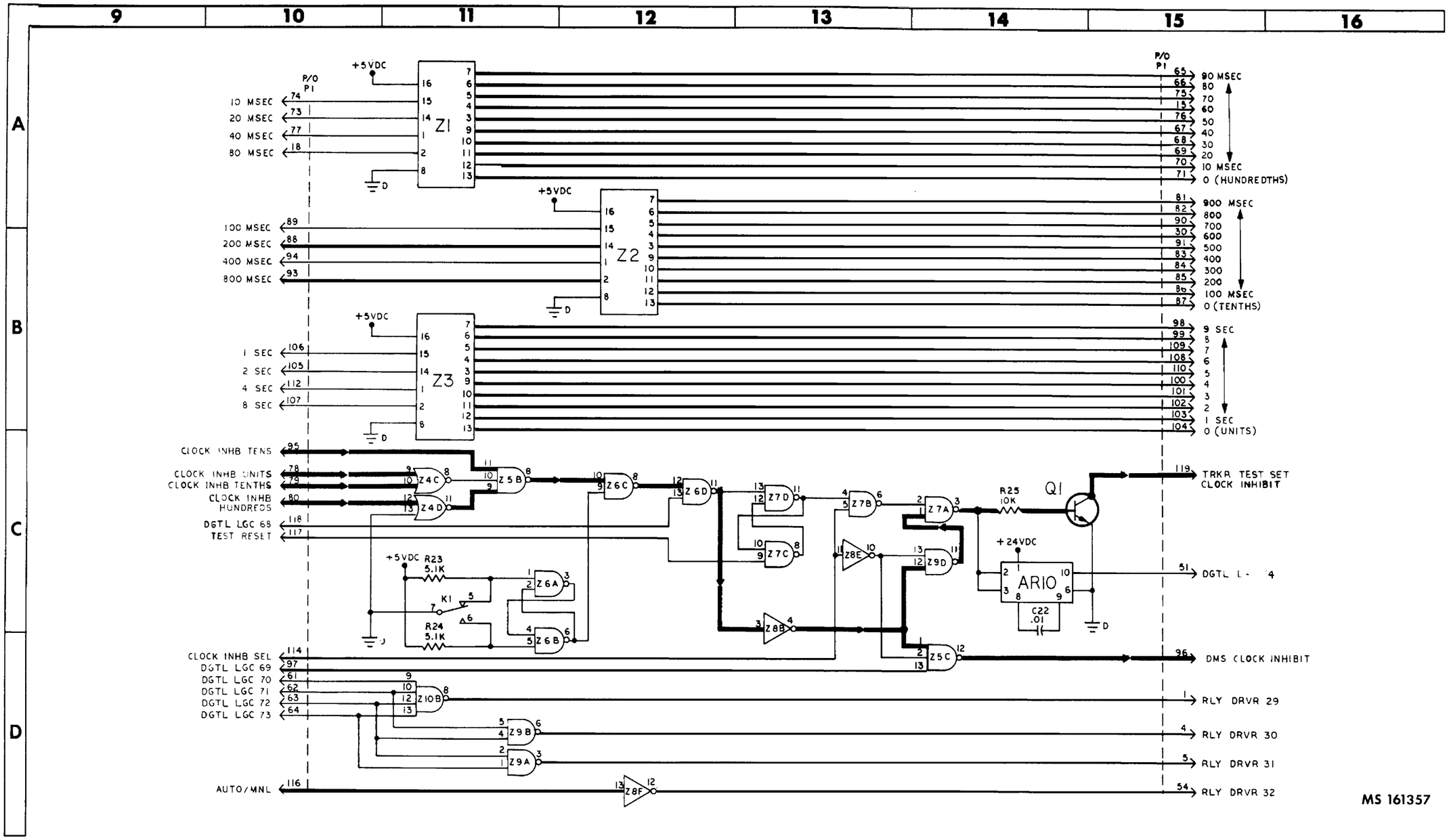


Figure 4-10. DMS-D card A9 (10275402) - schematic diagram (sheet 2 of 3)

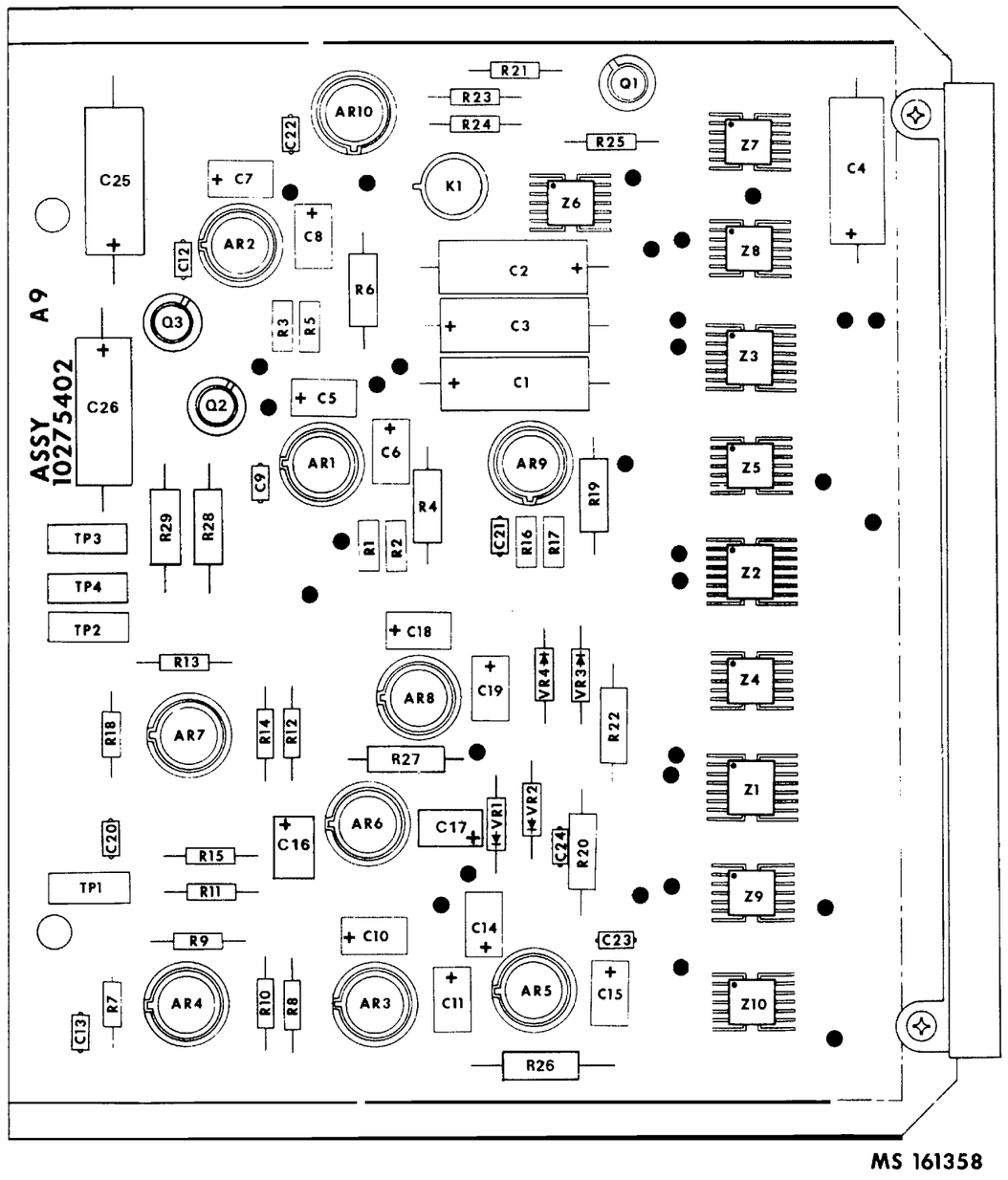


Figure 4-10. DMS-D card A9 (10275402) - schematic diagram (sheet 3 of 3)

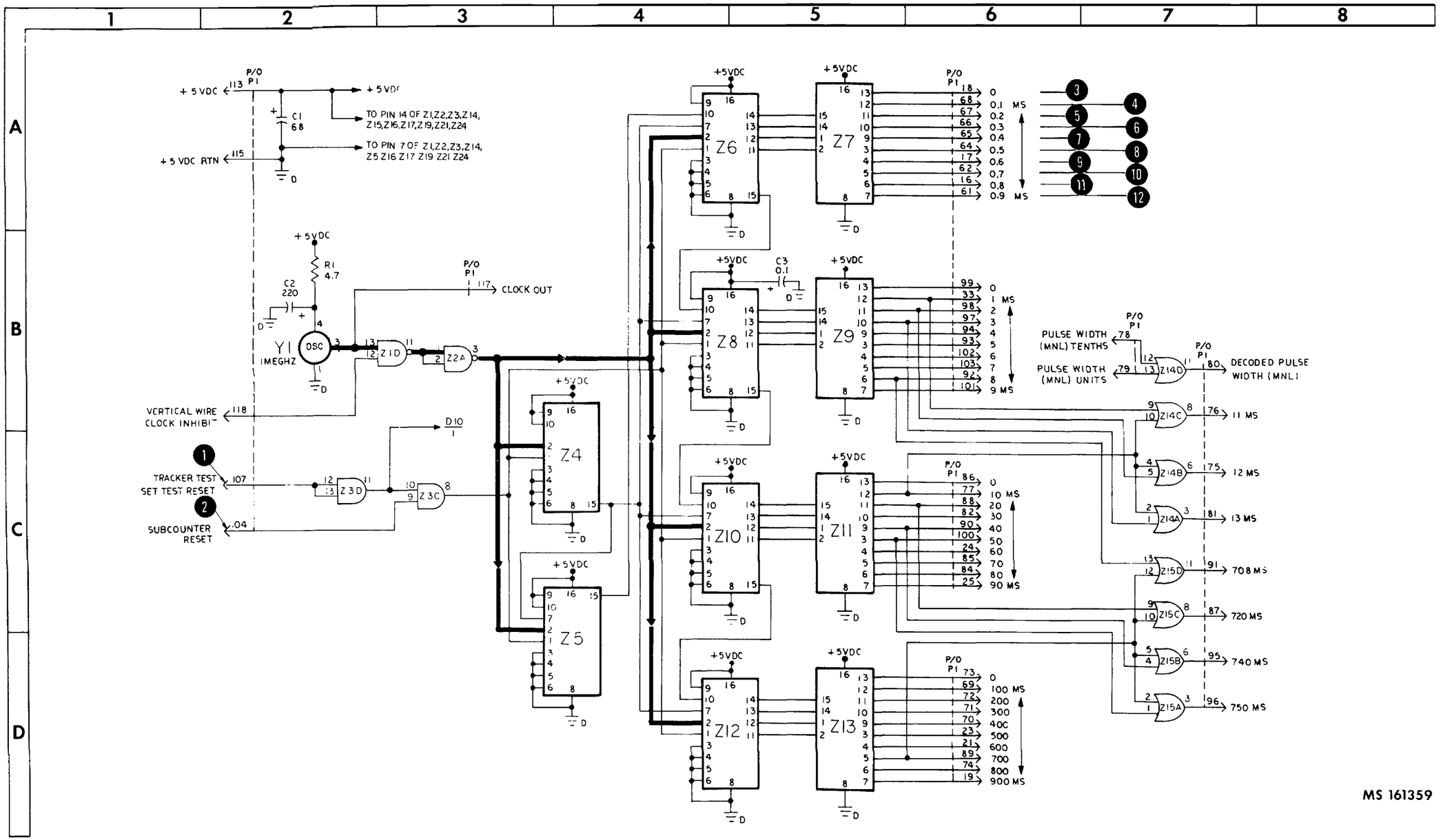


Figure 4-11. DMS-D card A10 schematic diagram (sheet 1 of 3)

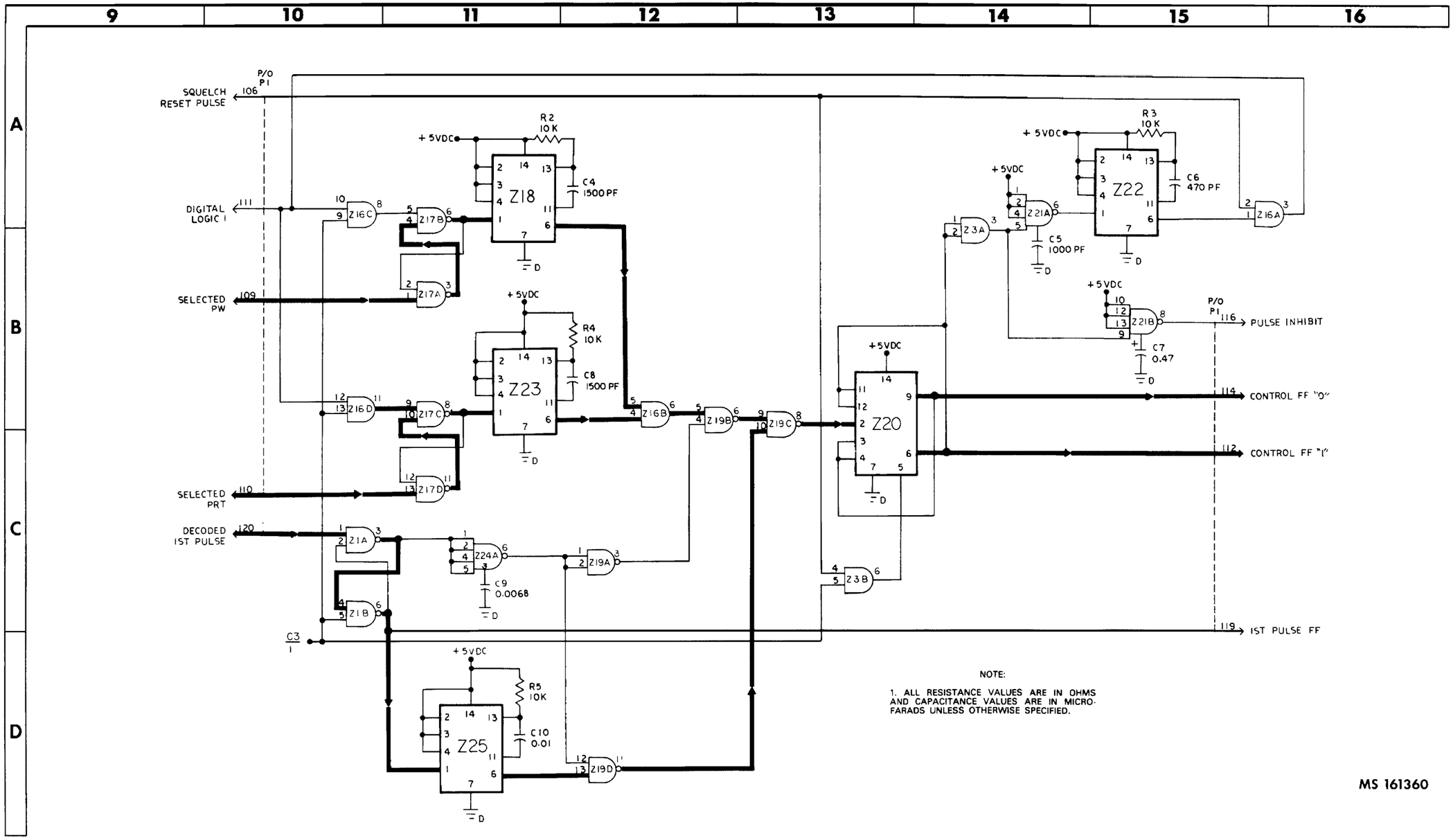
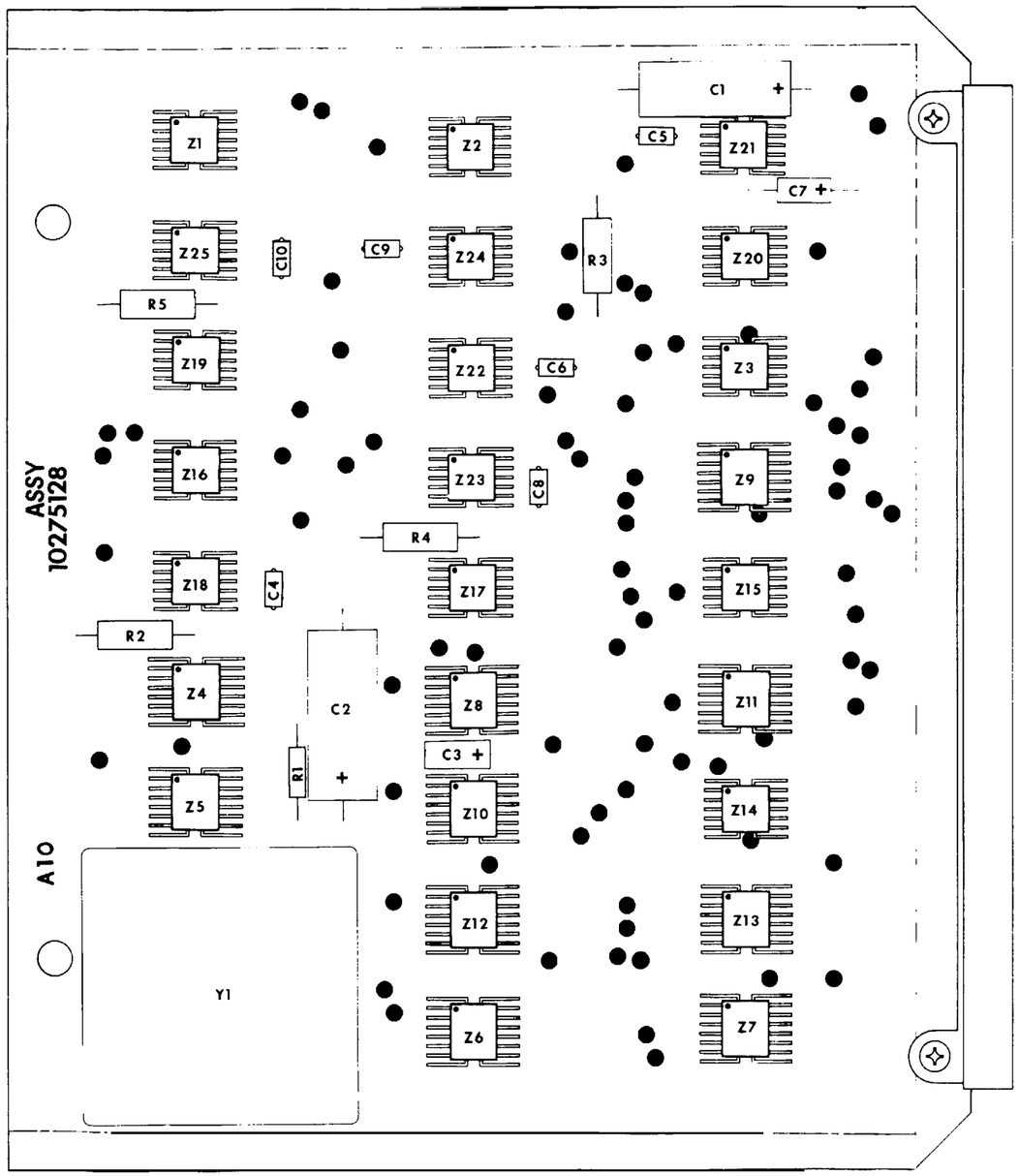
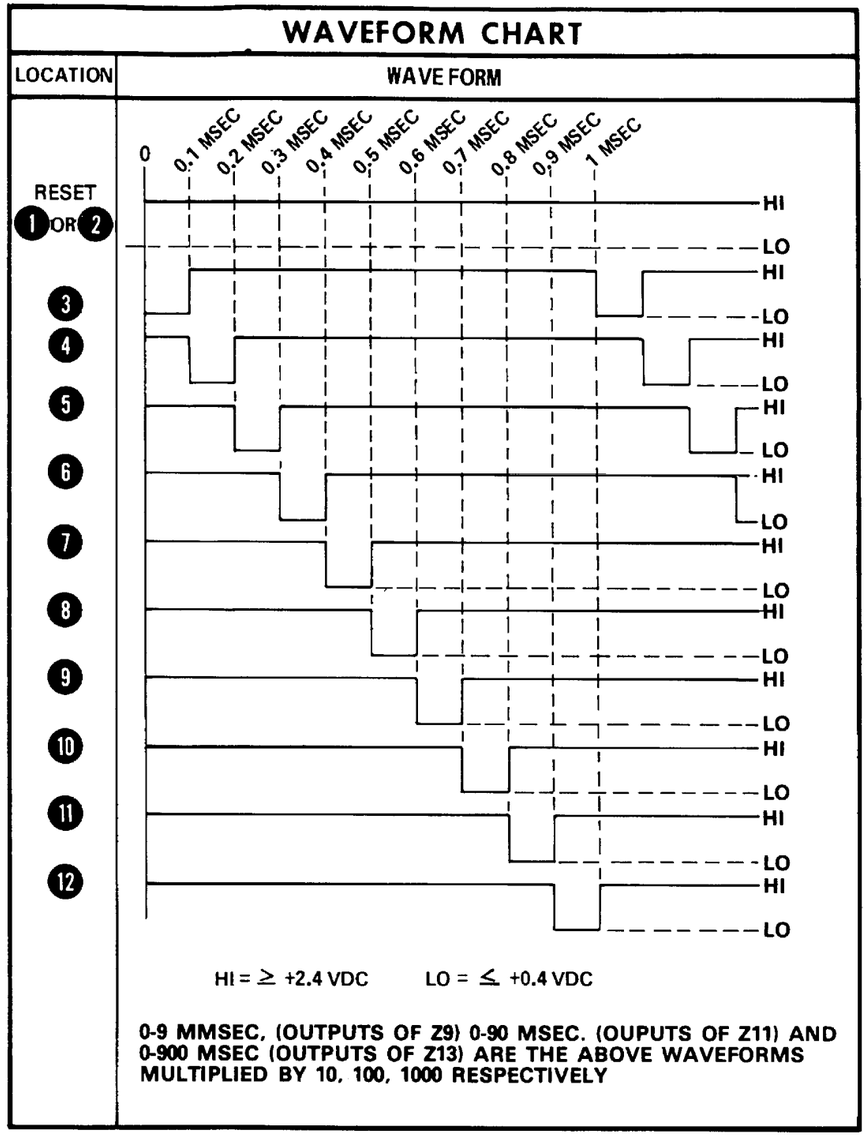


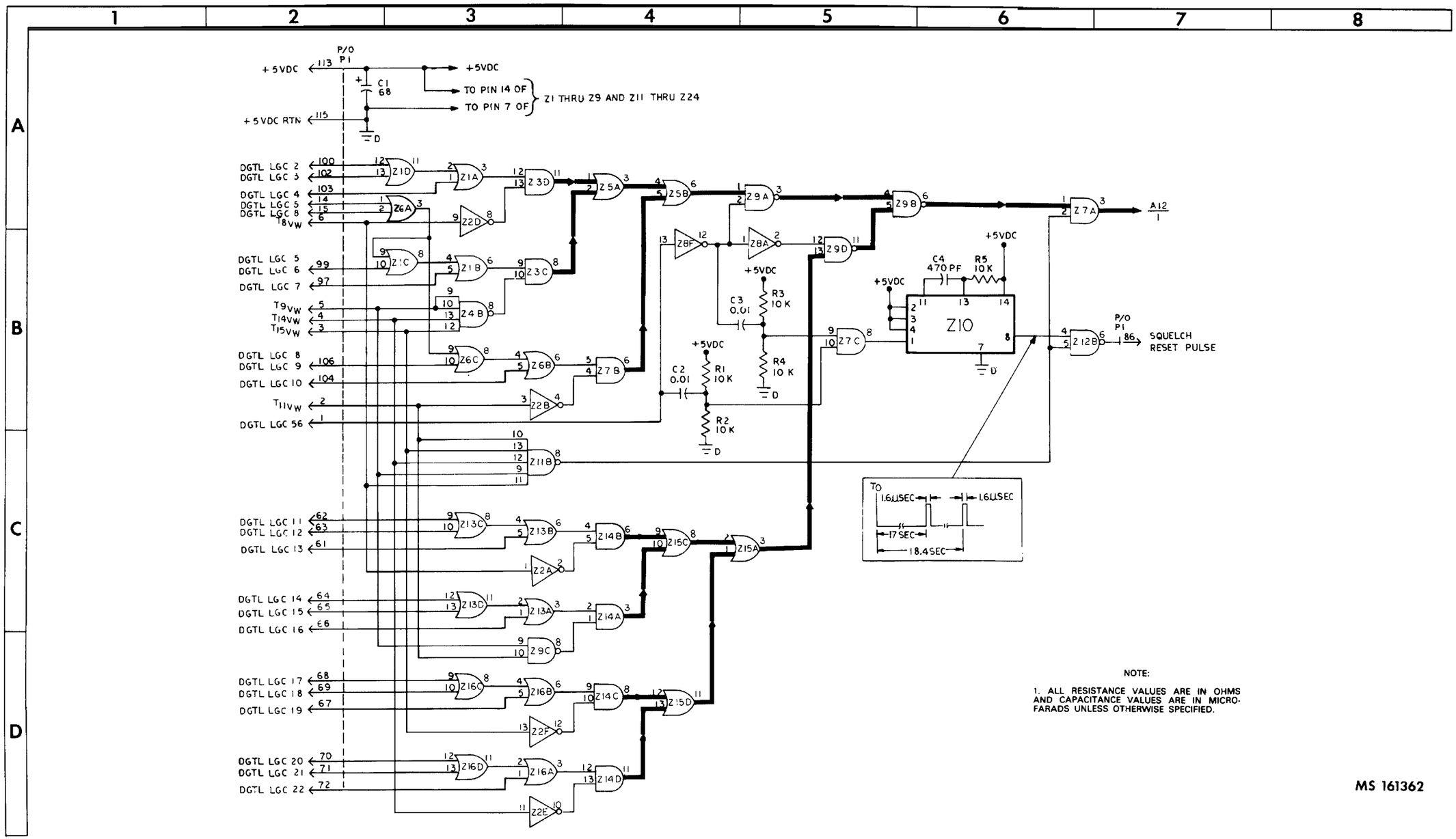
Figure 4-11. DMS-D card A10 schematic diagram (sheet 2 of 3)





MS 161361

Figure 4-11. DMS-D card A10 schematic diagram (sheet 3 of 3)



NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

MS 161362

Figure 4-12. DMS-D card All (10275131) - schematic diagram (sheet 1 of 4)

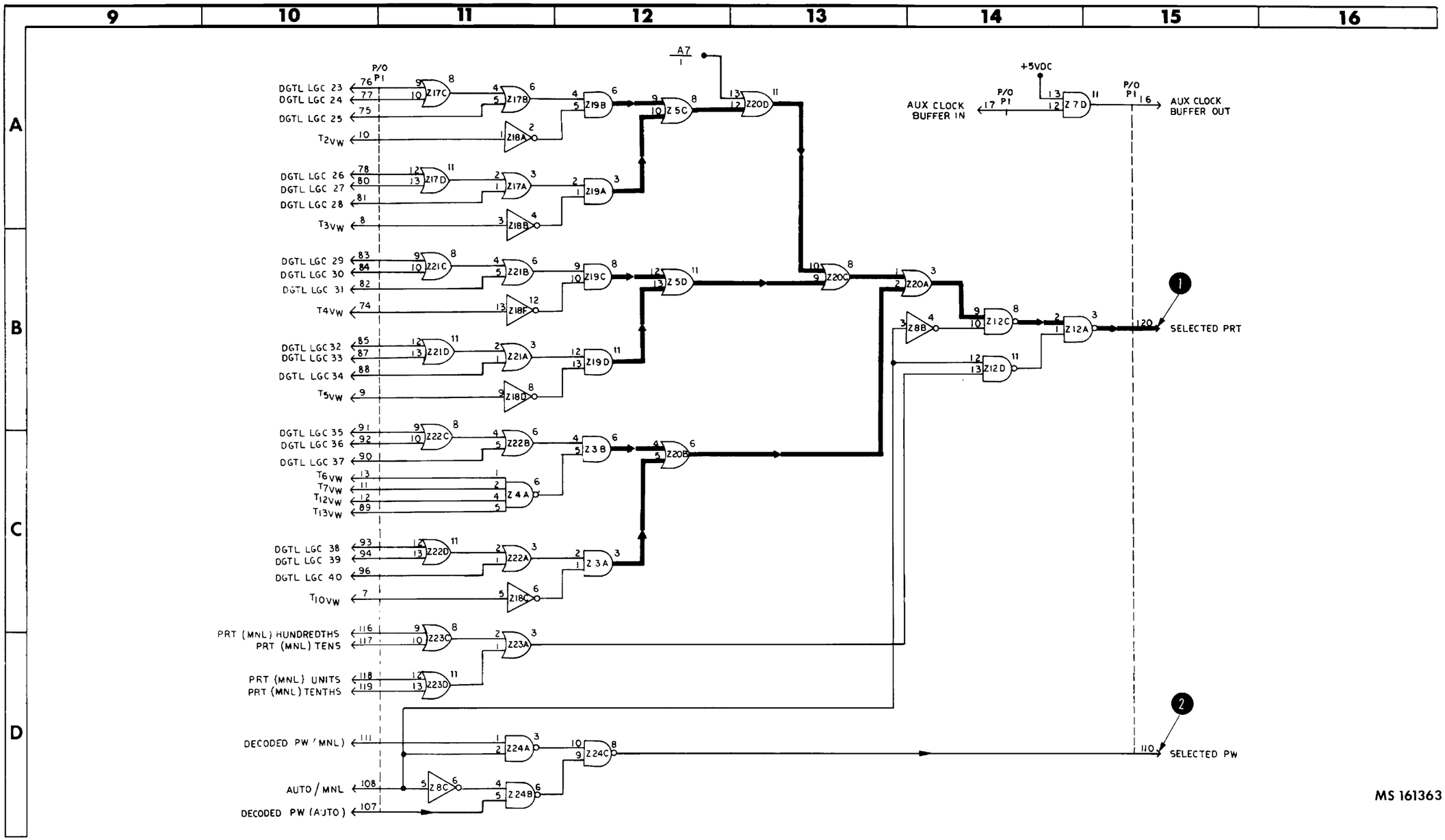
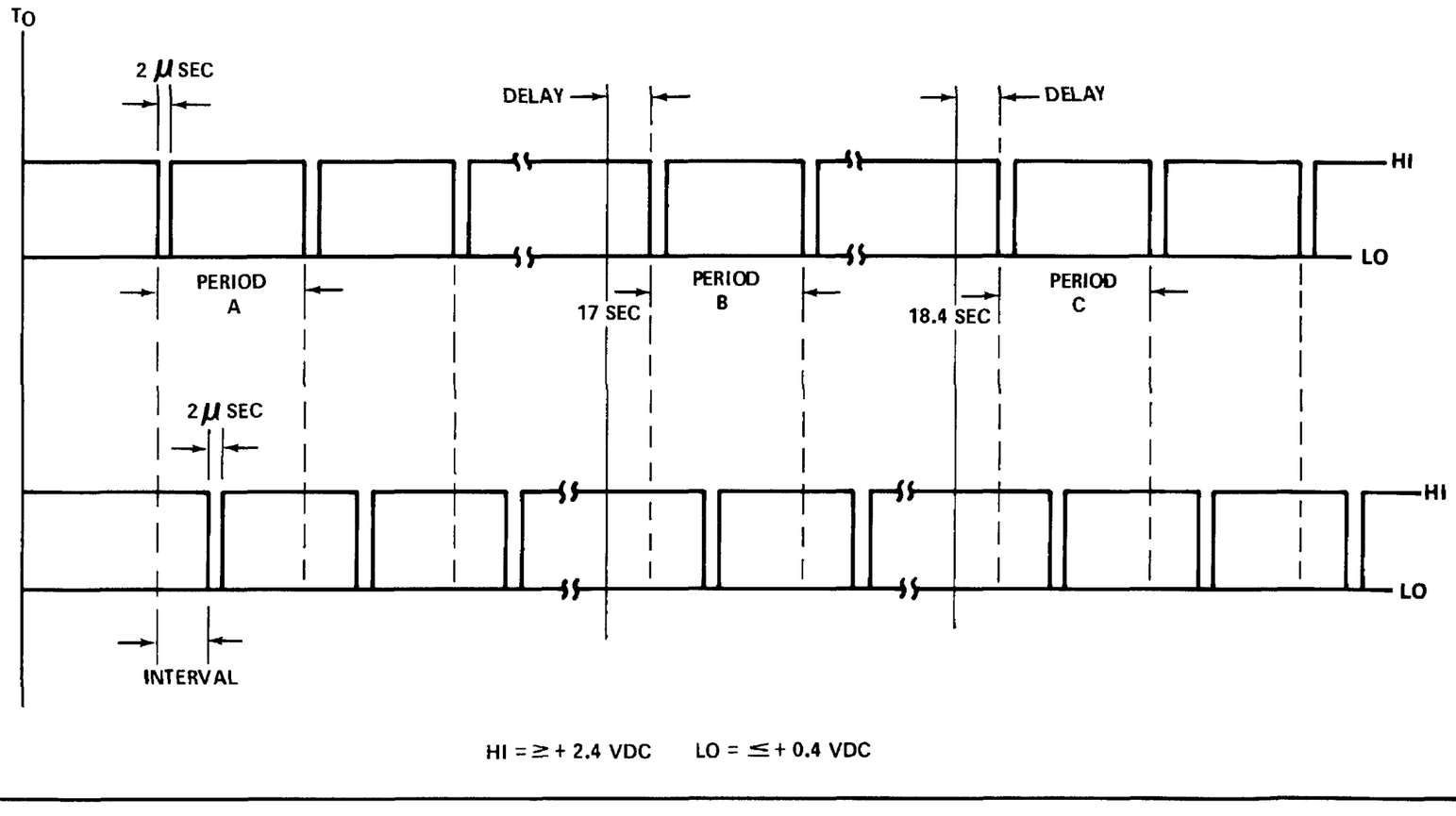


Figure 4-12. DMS-D card All (10275131) - schematic diagram (sheet 2 of 4)

WAVEFORM CHART

LOCATION	WAVEFORM



HI = ≥ + 2.4 VDC LO = ≤ + 0.4 VDC

FUNCTION TABLE

SEQUENCE SWITCH POSITION	PERIOD A (MSEC)	PERIOD B (MSEC)	PERIOD C (MSEC)	DELAY (MSEC)	INTERVAL (MSEC)
2	308	308	308	—	10
3	427	427	427	—	10
4	302	302	302	—	9.1
5	435	435	435	—	8.9
6	333	333	333	—	10
7	333	333	333	—	10
8	85.6	358	85.6	10	10
9	171.3	249	171.3	9.1	9.1
10	84	84	84	—	10
11	174.7	249	174.7	10	10
12	333	333	333	—	10
13	333	333	333	—	10
14	171.3	365	171.3	10	10
15	171.3	244	171.3	10	10

MS 161364

Figure 4-12. DMS-D card All (10275131) - schematic diagram (sheet 3 of 4)

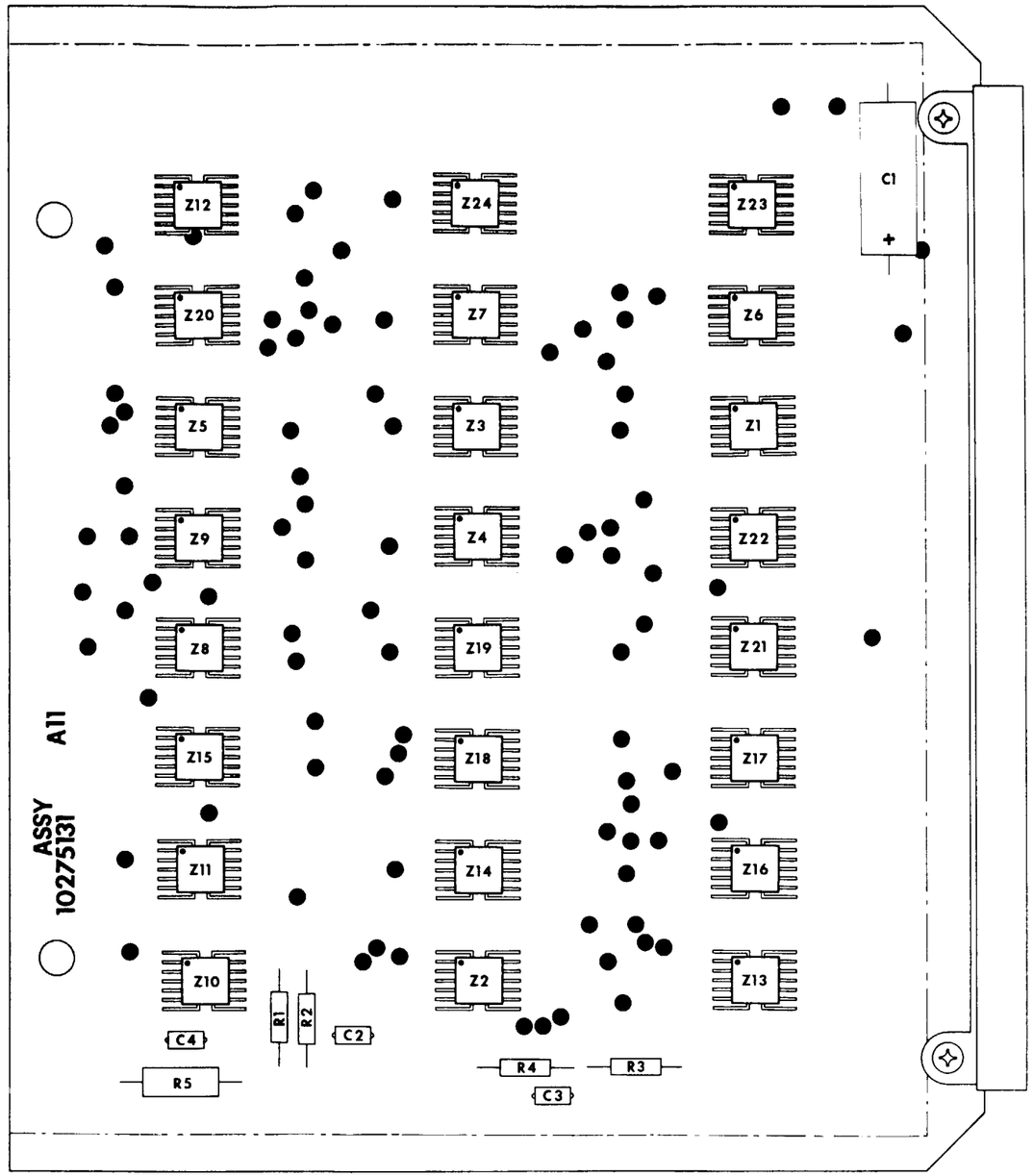


Figure 4-12. DMS-D card All (10275131)-schematic diagram (sheet 4 of 4)

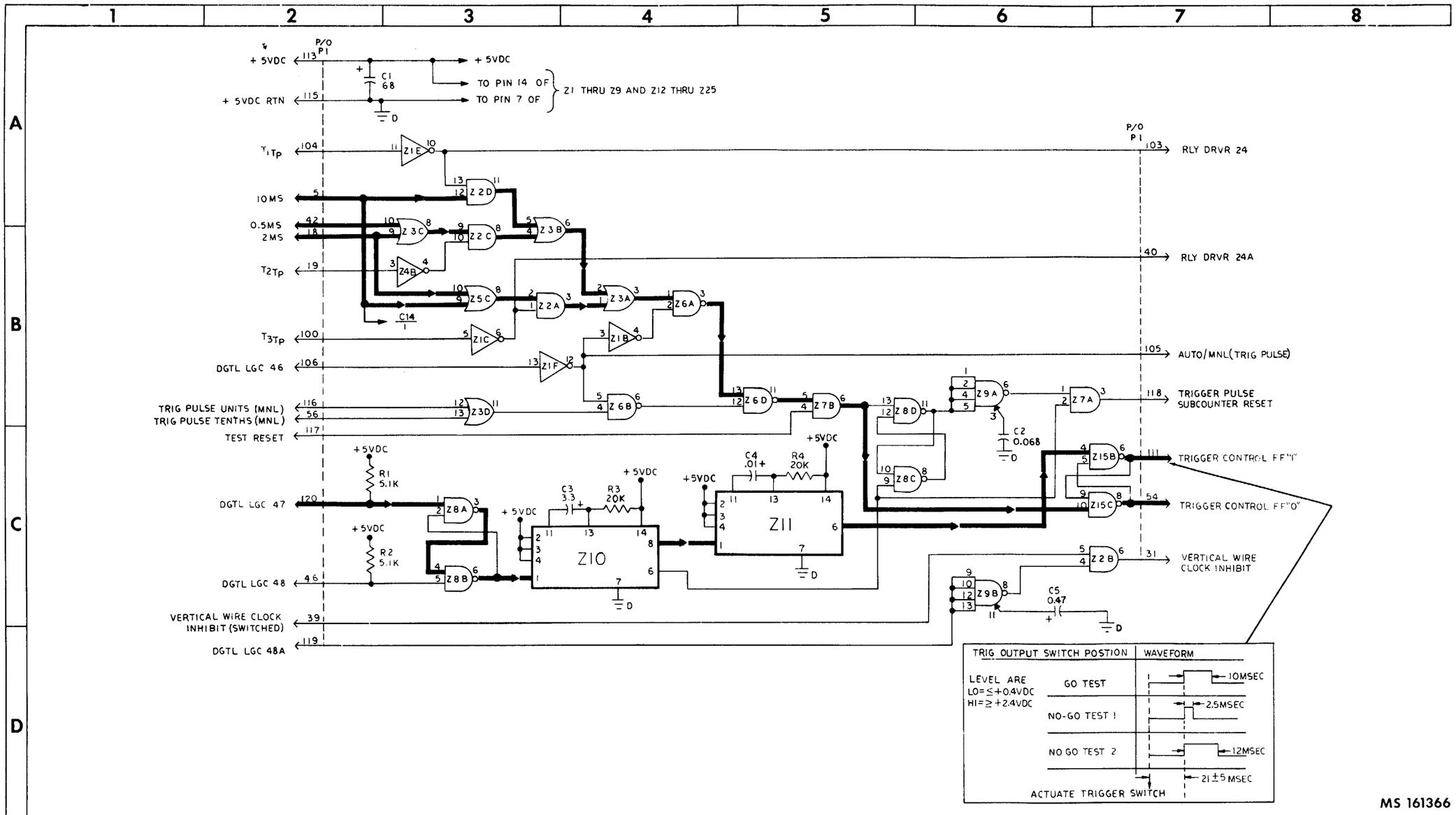
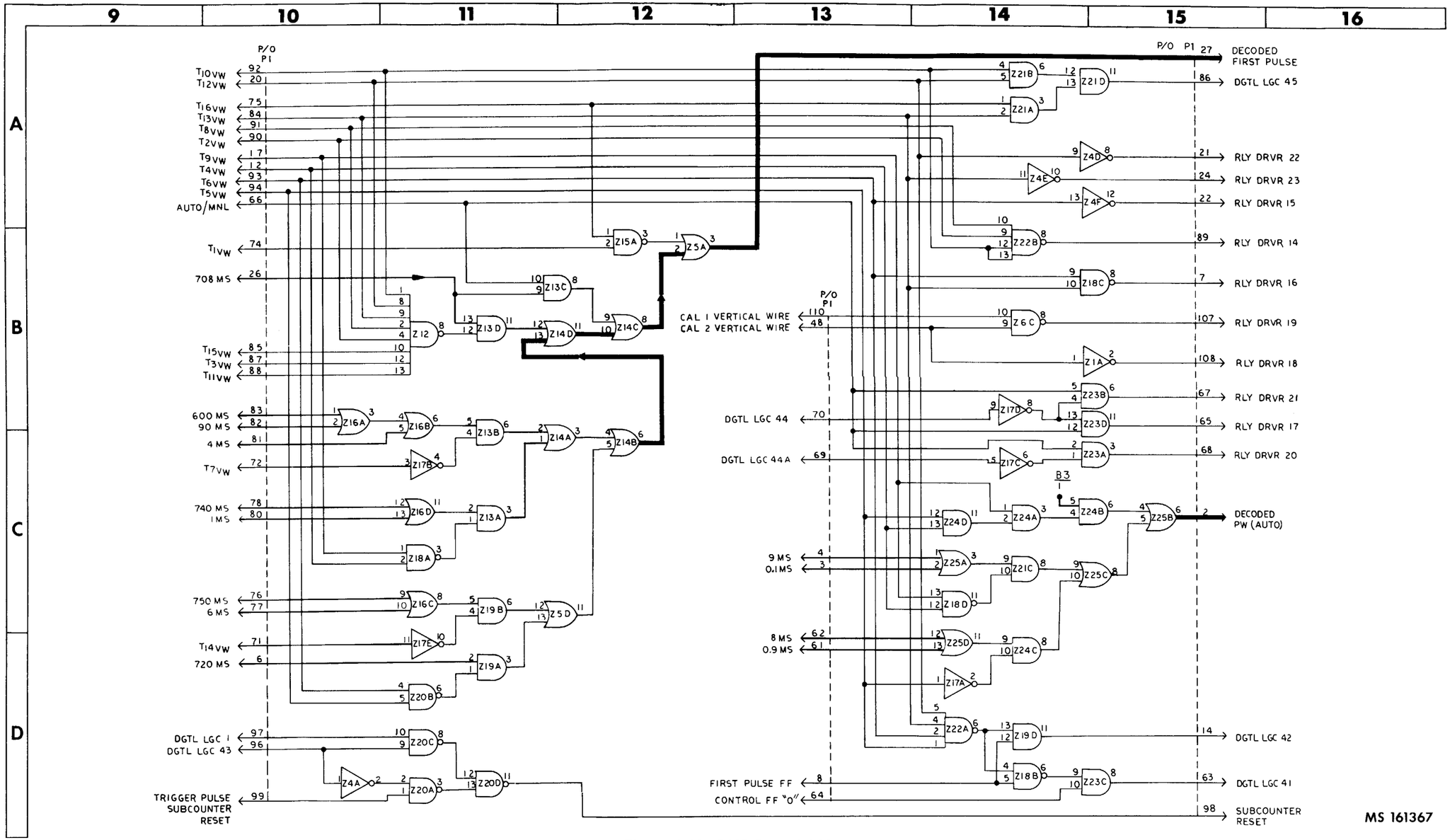


Figure 4-13. DMS-D card A12 (10275140) - schematic diagram (sheet 1 of 3)



MS 161367

Figure 4-13. DMS-D card A12 schematic diagram (sheet 2 of 3)

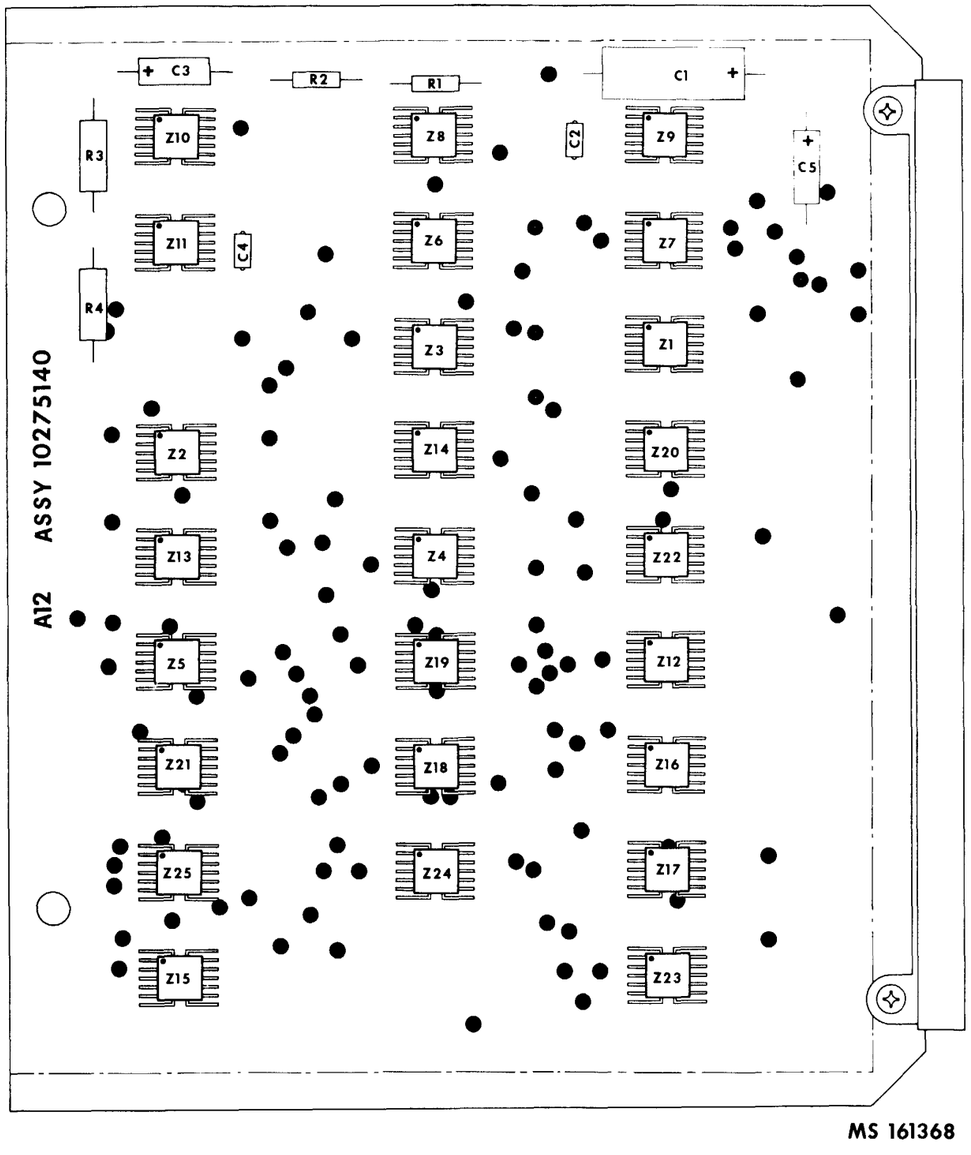


Figure 4-13. DMS-D card A12 schematic diagram (sheet 3 of 3)

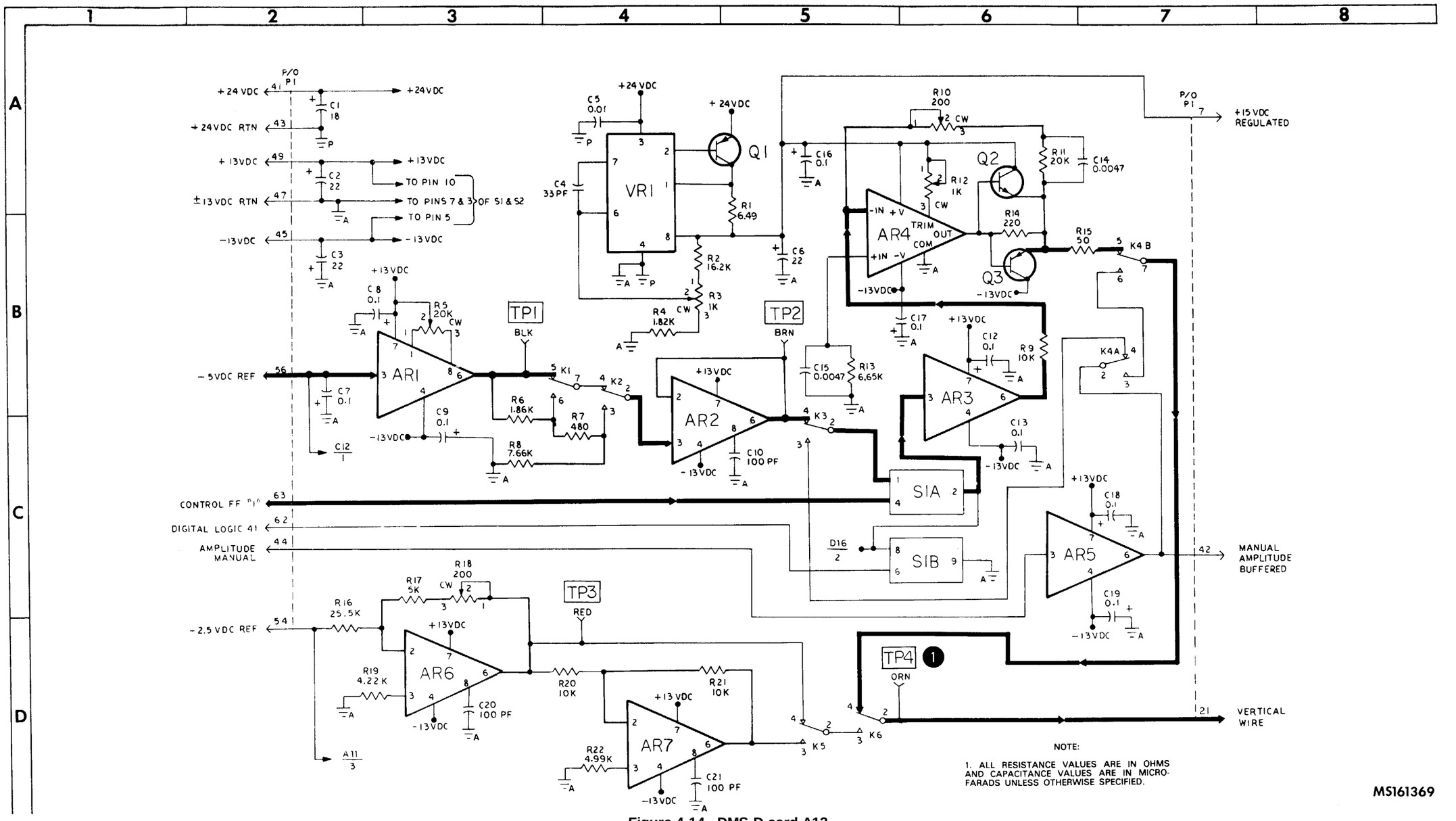


Figure 4-14. DMS-D card A13 schematic diagram (sheet 1 of 4)

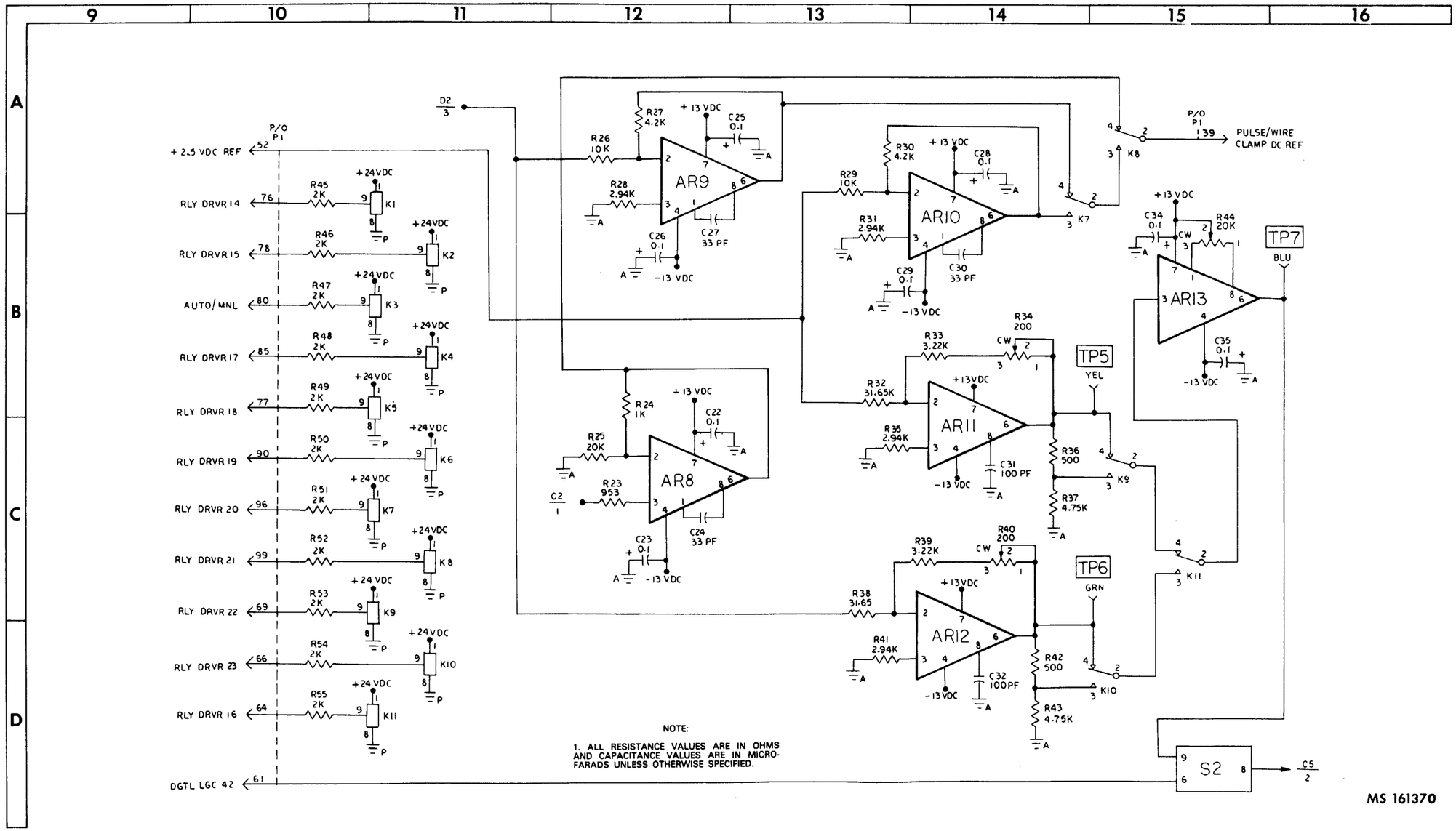
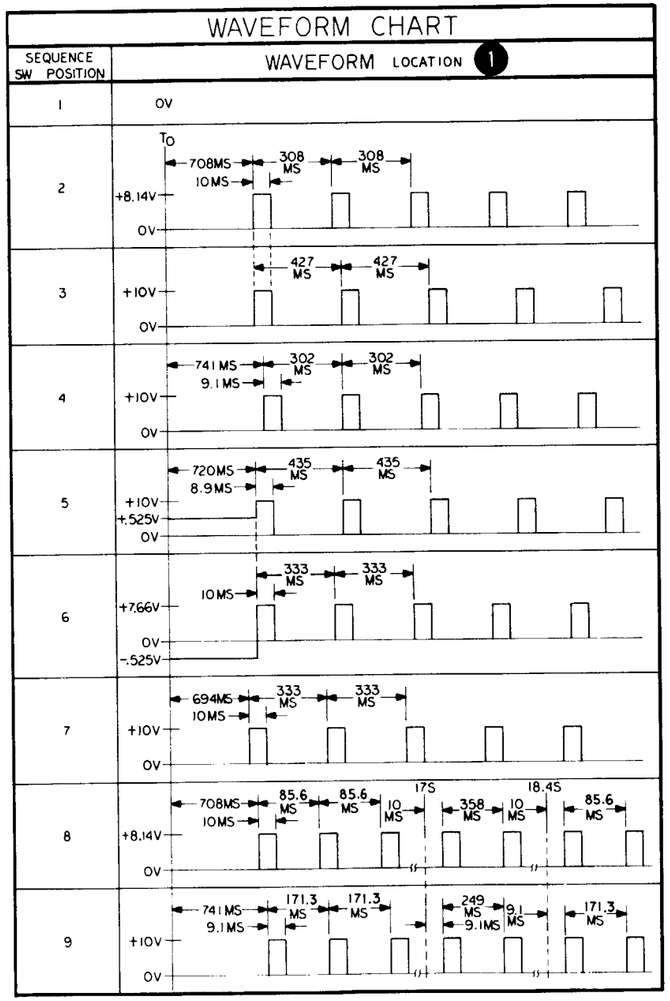
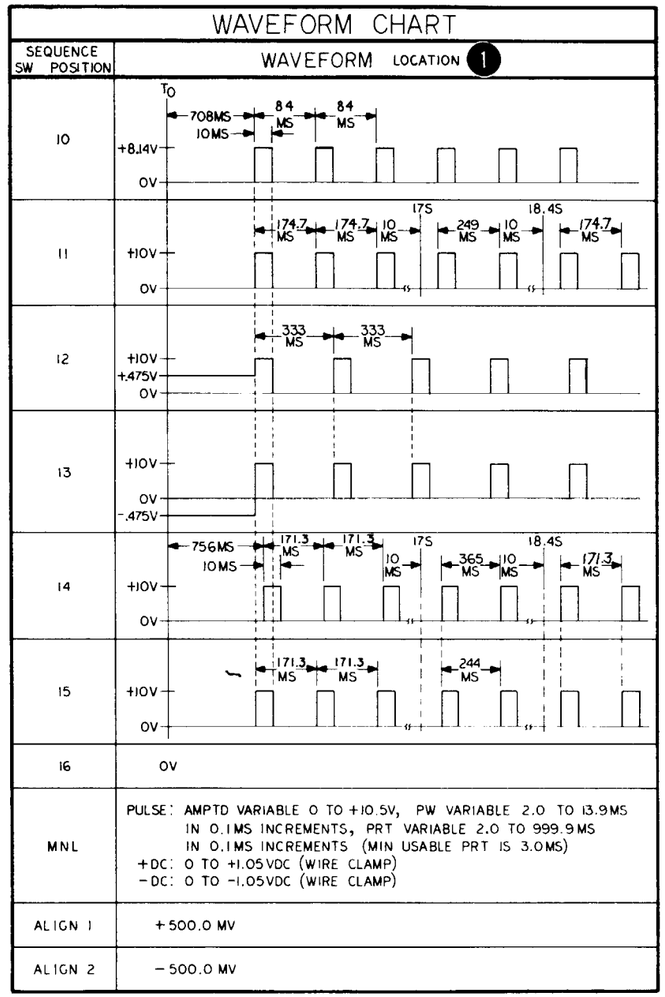


Figure 4-14. DMS-D card A13 - schematic diagram (sheet 2 of 4)





MS 161371

Figure 4-14. DMS-D card A13 - schematic diagram (sheet 3 of 4)

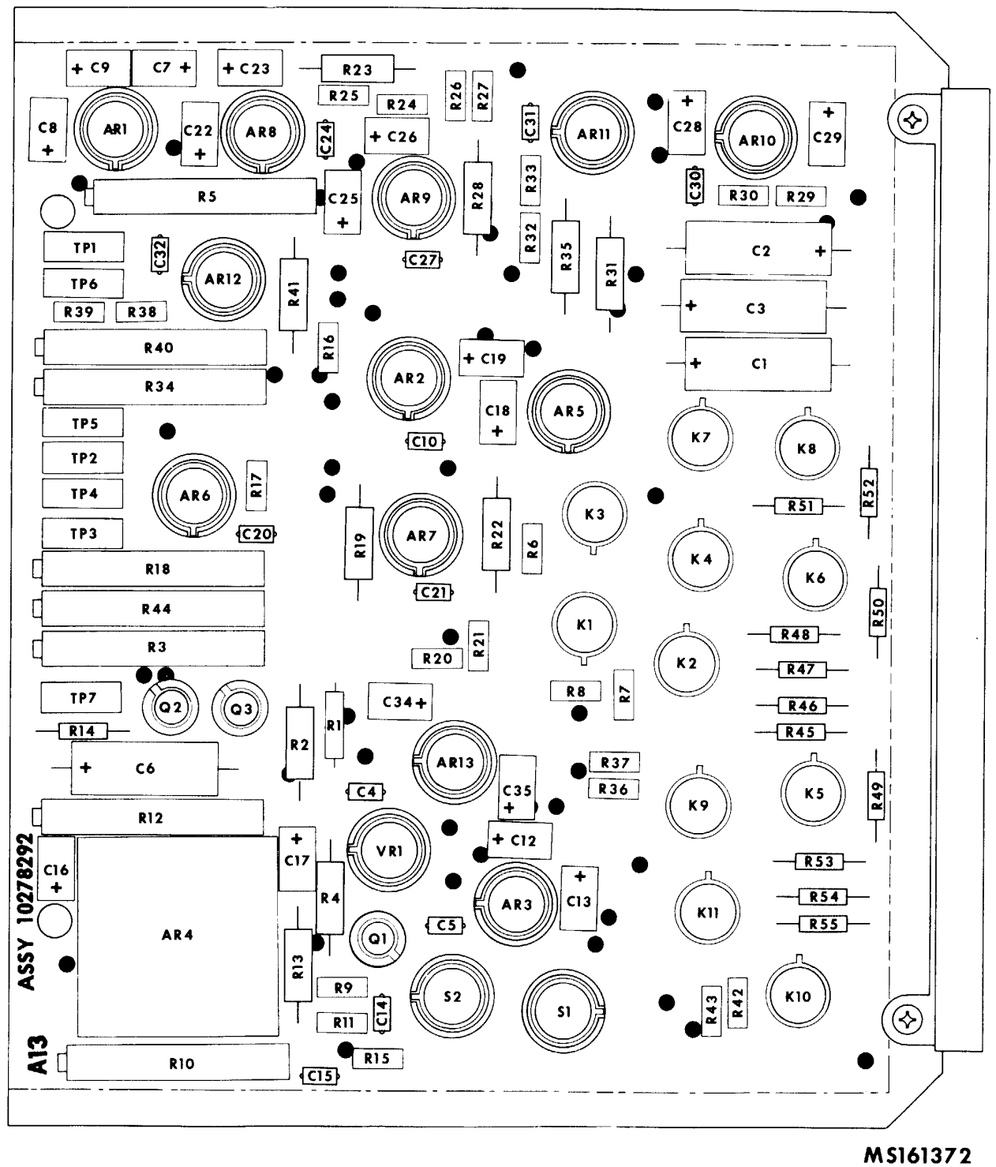
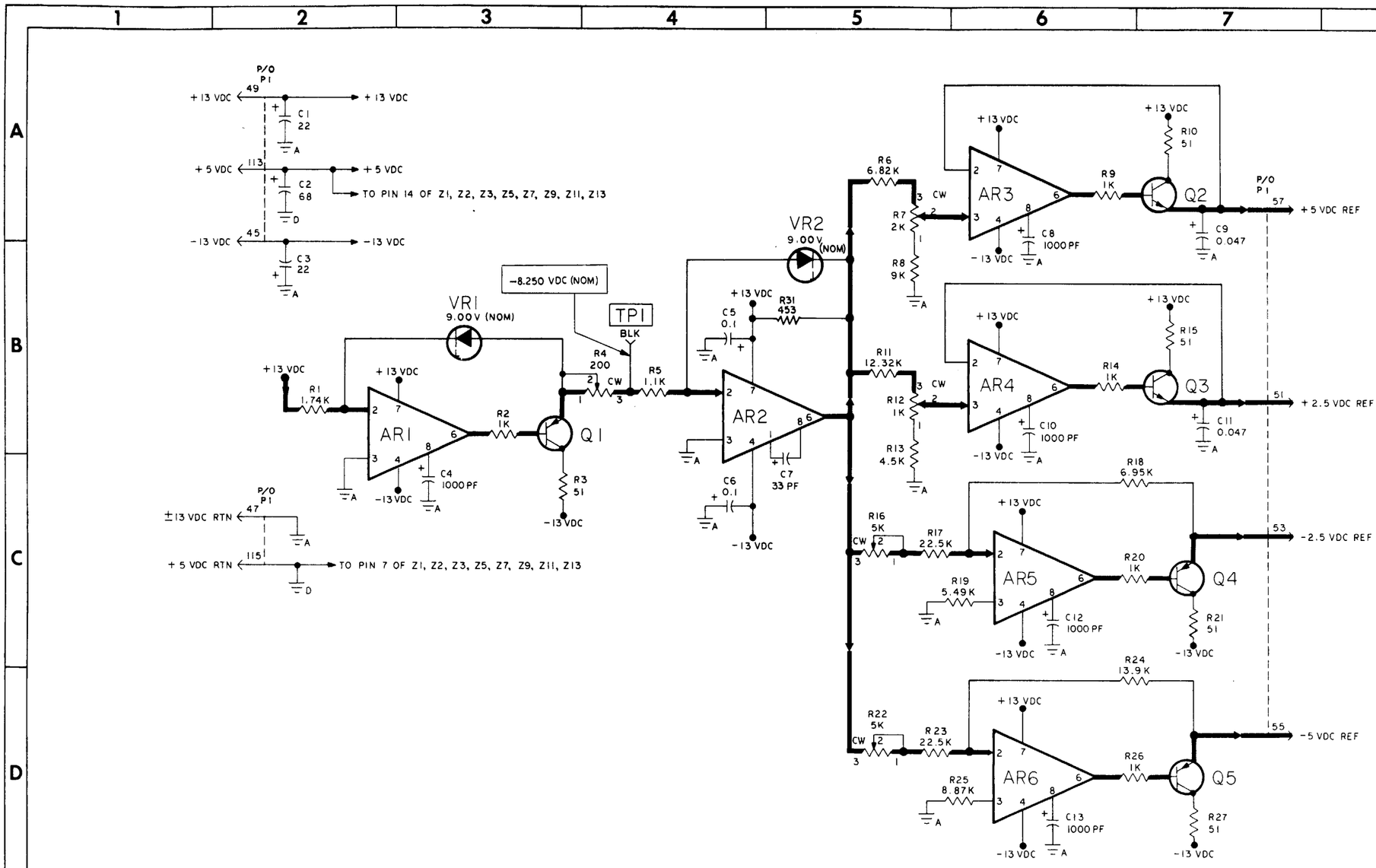


Figure 4-14. DMS-D card A13 - schematic diagram (sheet 4 of 4)



MS 161373

Figure 4-15. DMS-D card A14 (10275092)-schematic diagram (sheet 1 of 3)

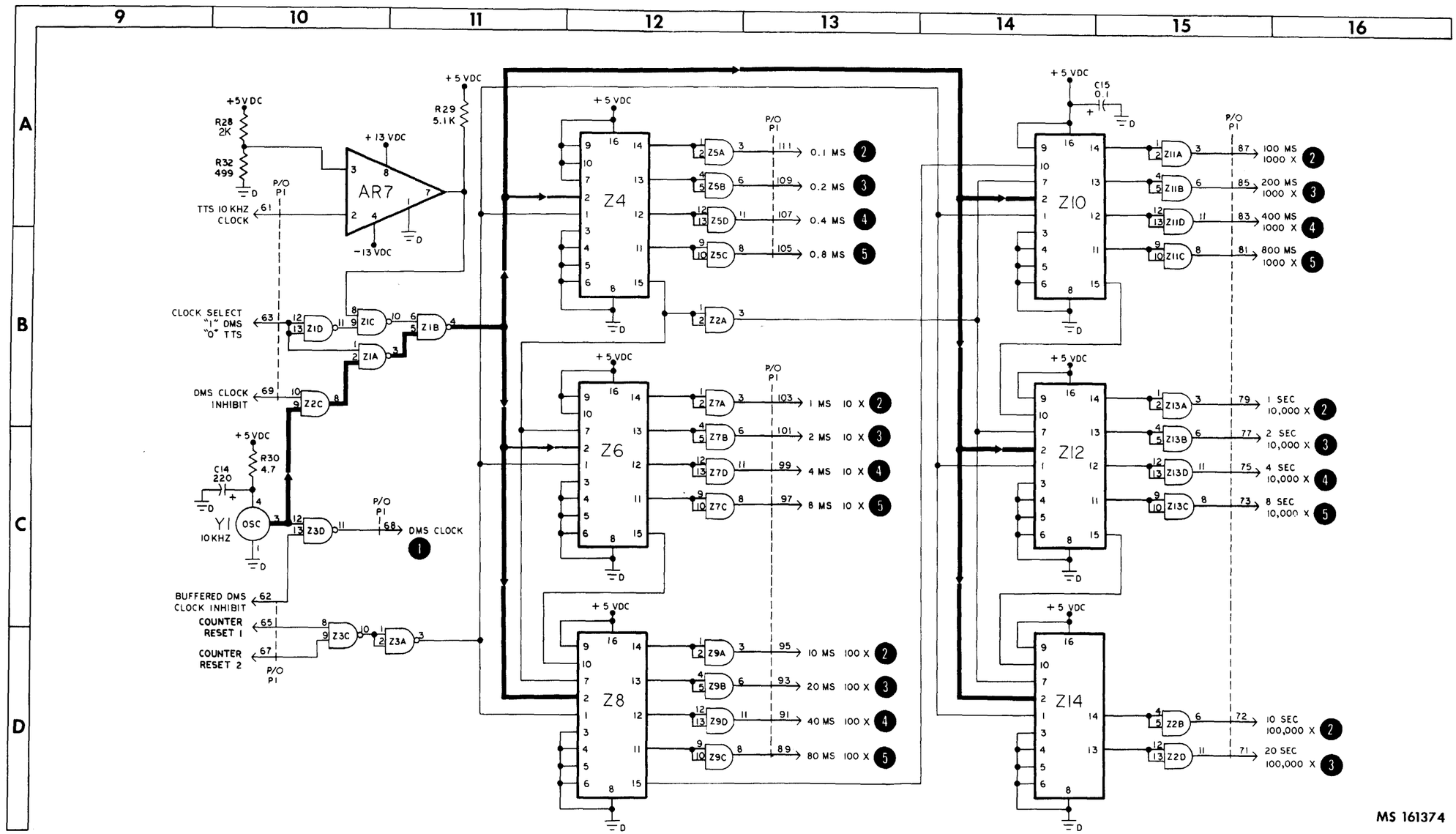
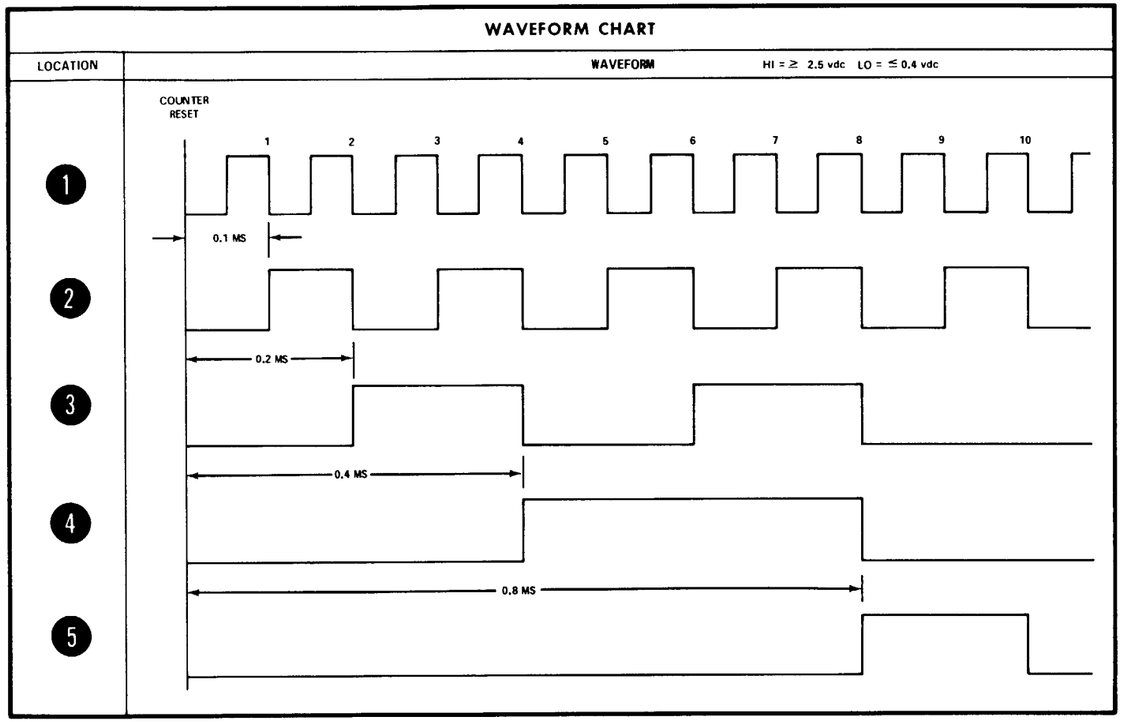


Figure 4-15. DMS-D card A14 (10275092) - schematic diagram (sheet 2 of 3)



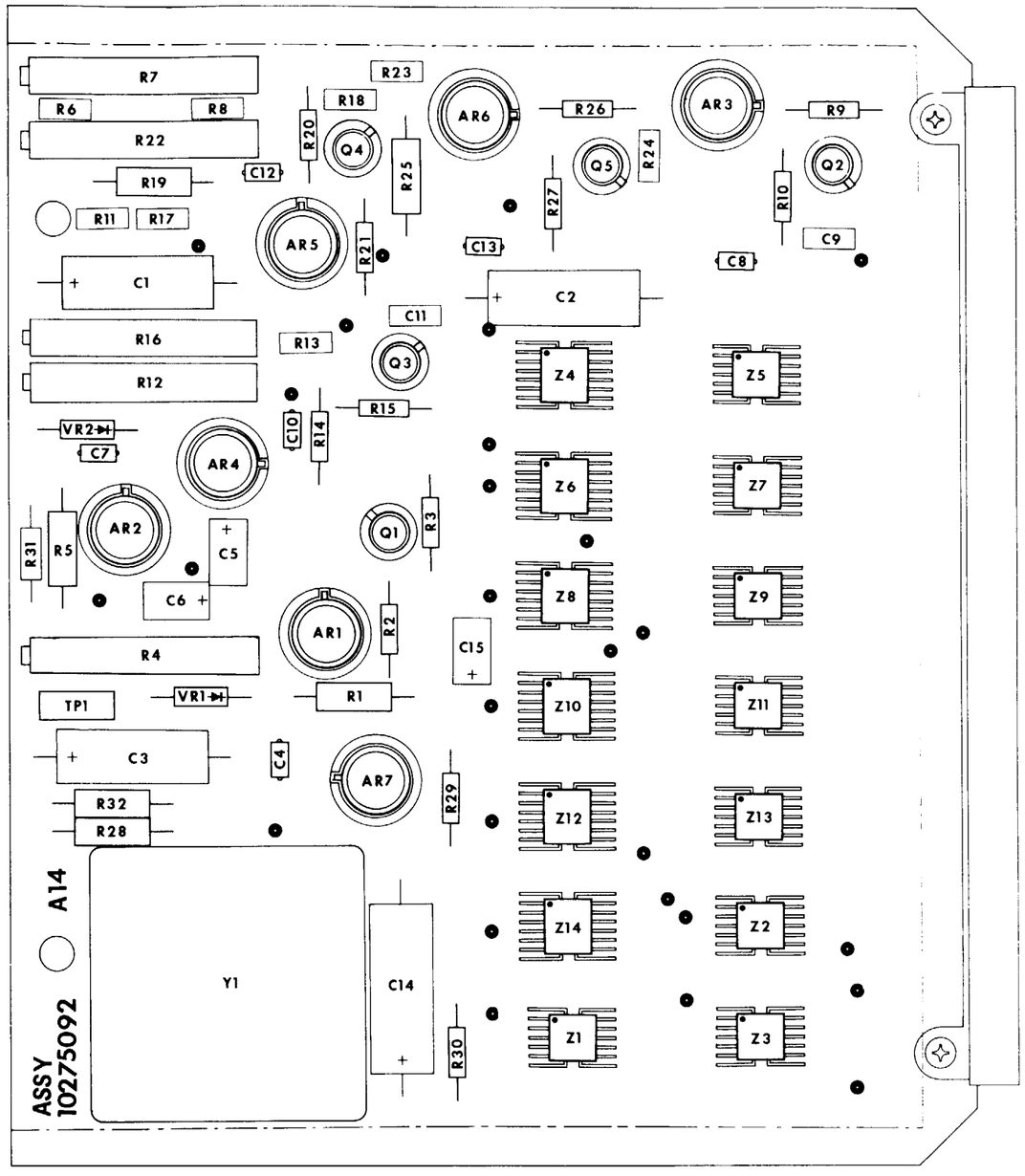


Figure 4-15. DMS-D card A14 (10275092 -schematic diagram (sheet 3 of 3)

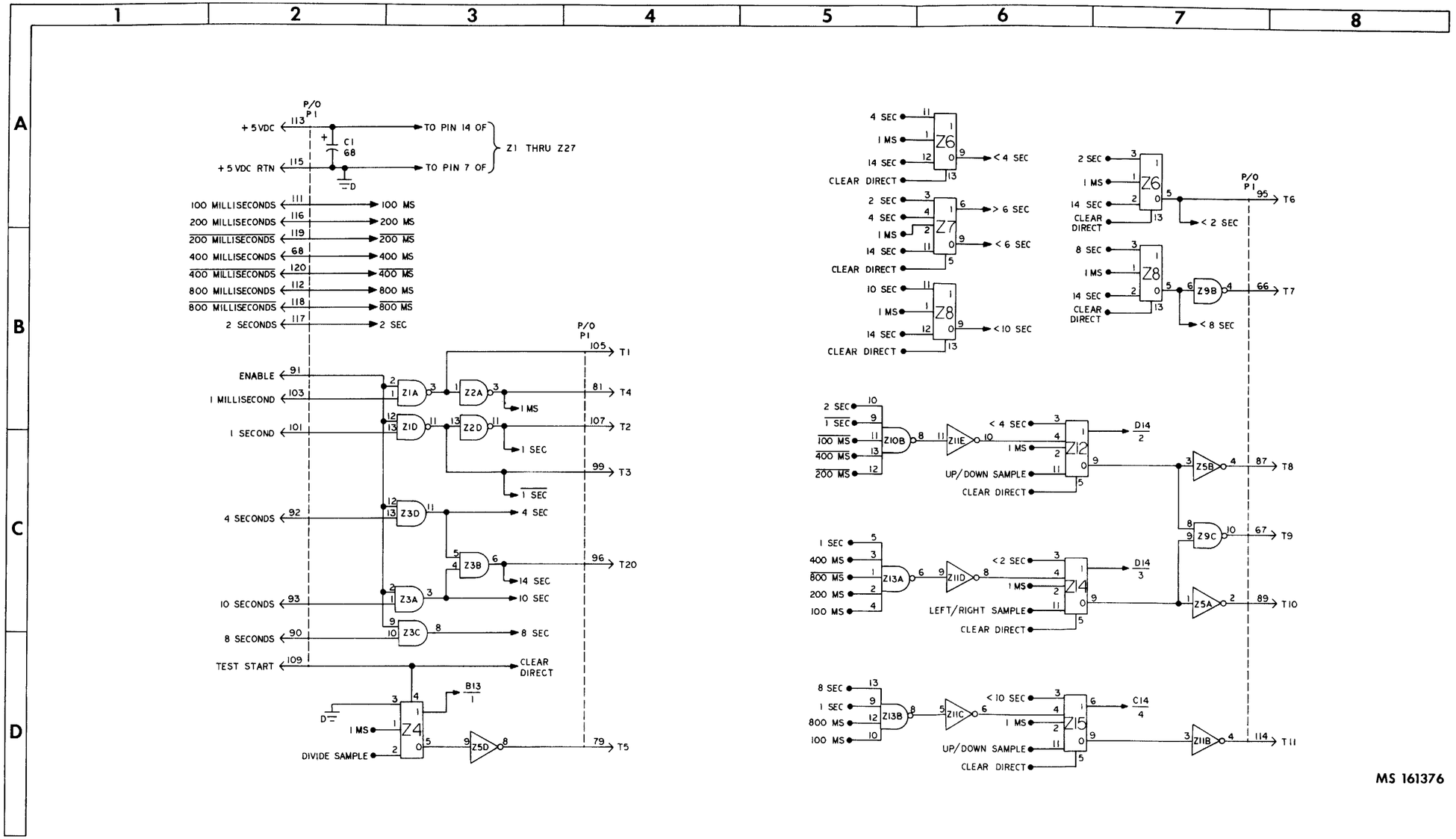
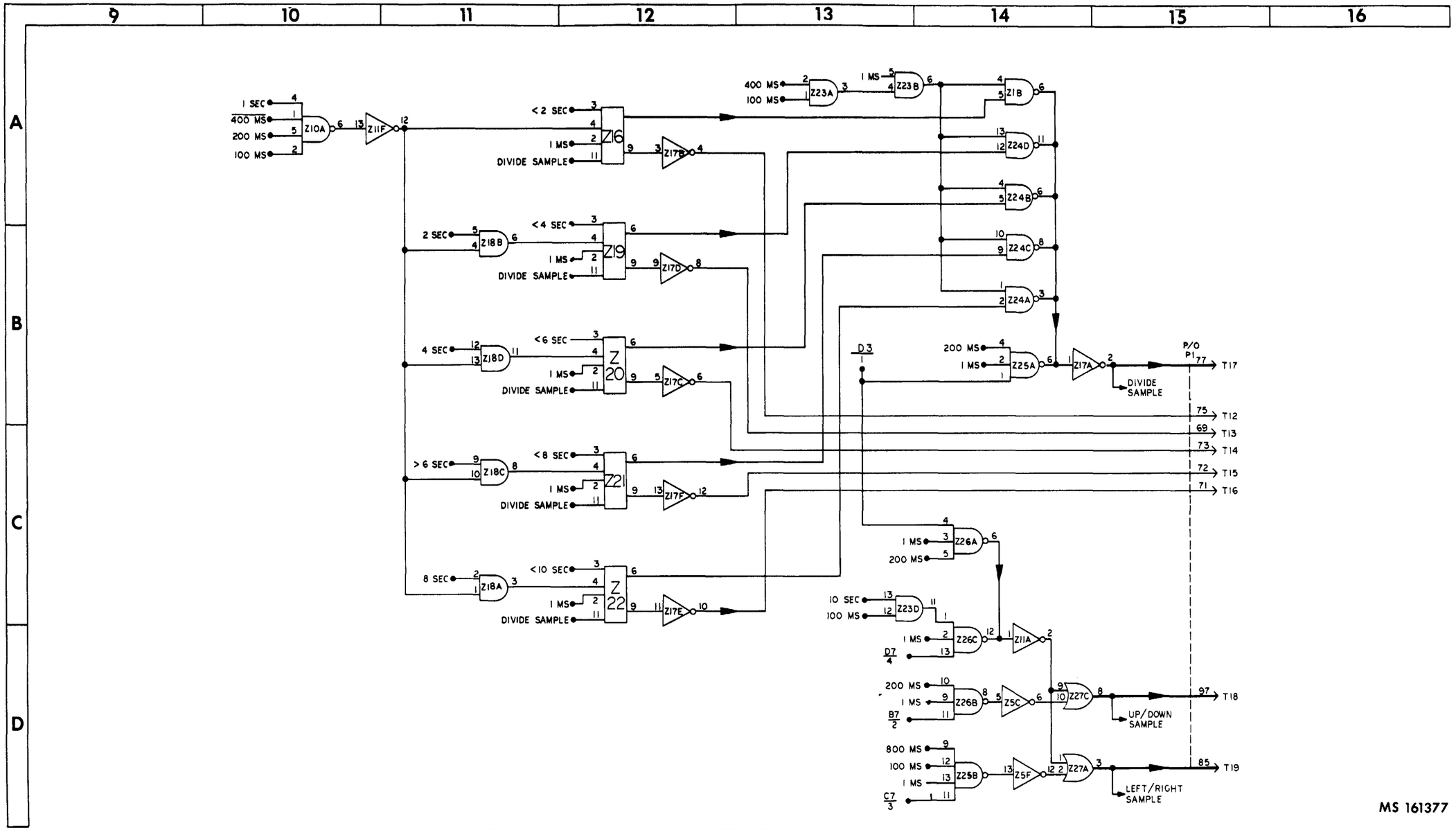


Figure 4-16. DMS-D card A15 (10275107)-schematic diagram (sheet 1 of 3)



MS 161377

Figure 4-16. DMS-D card A15 (10275107)- schematic diagram (sheet 2 of 3)

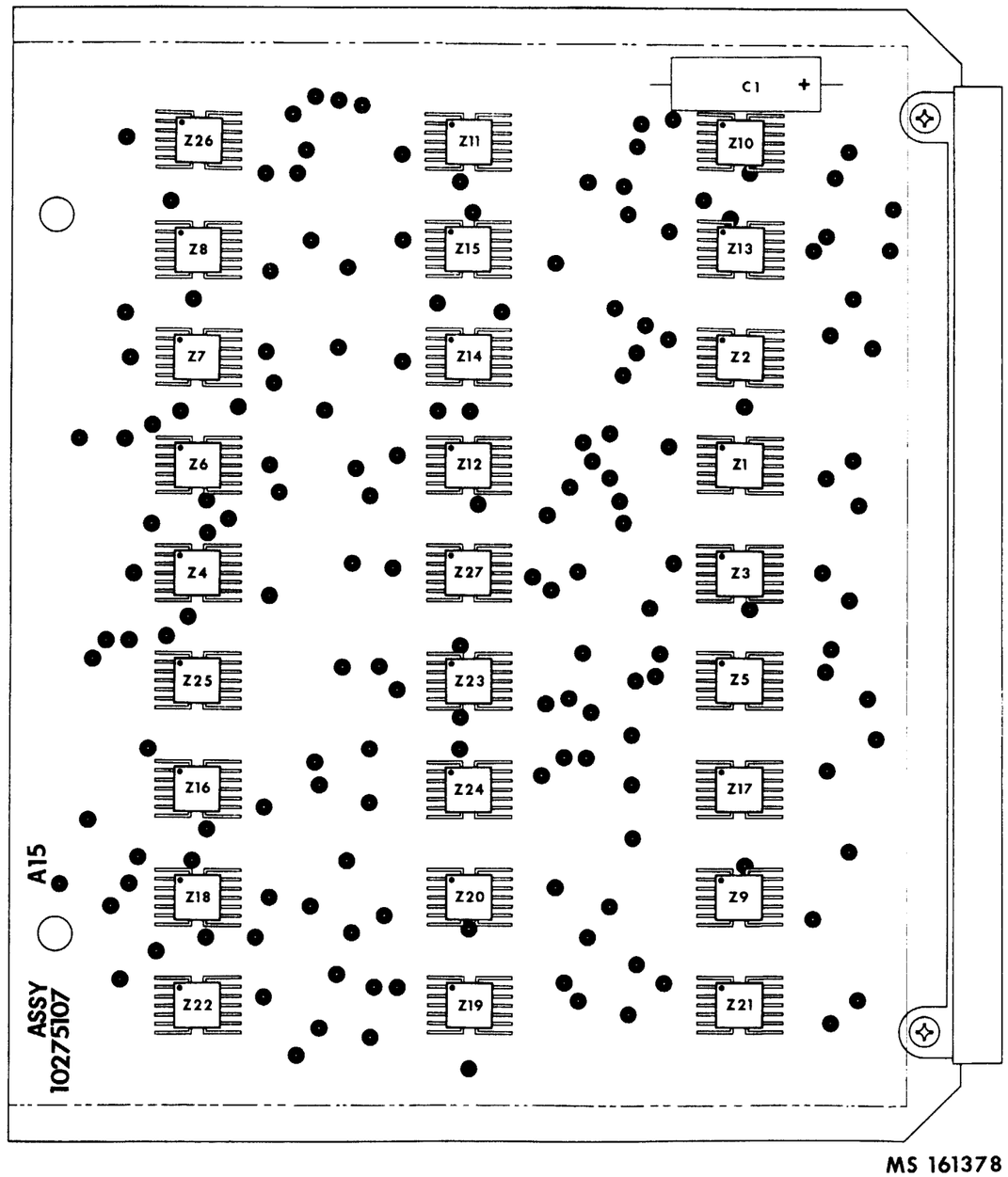


Figure 4-16. DMS-D card A15 (10275107)-schematic diagram (sheet 3 of 3)

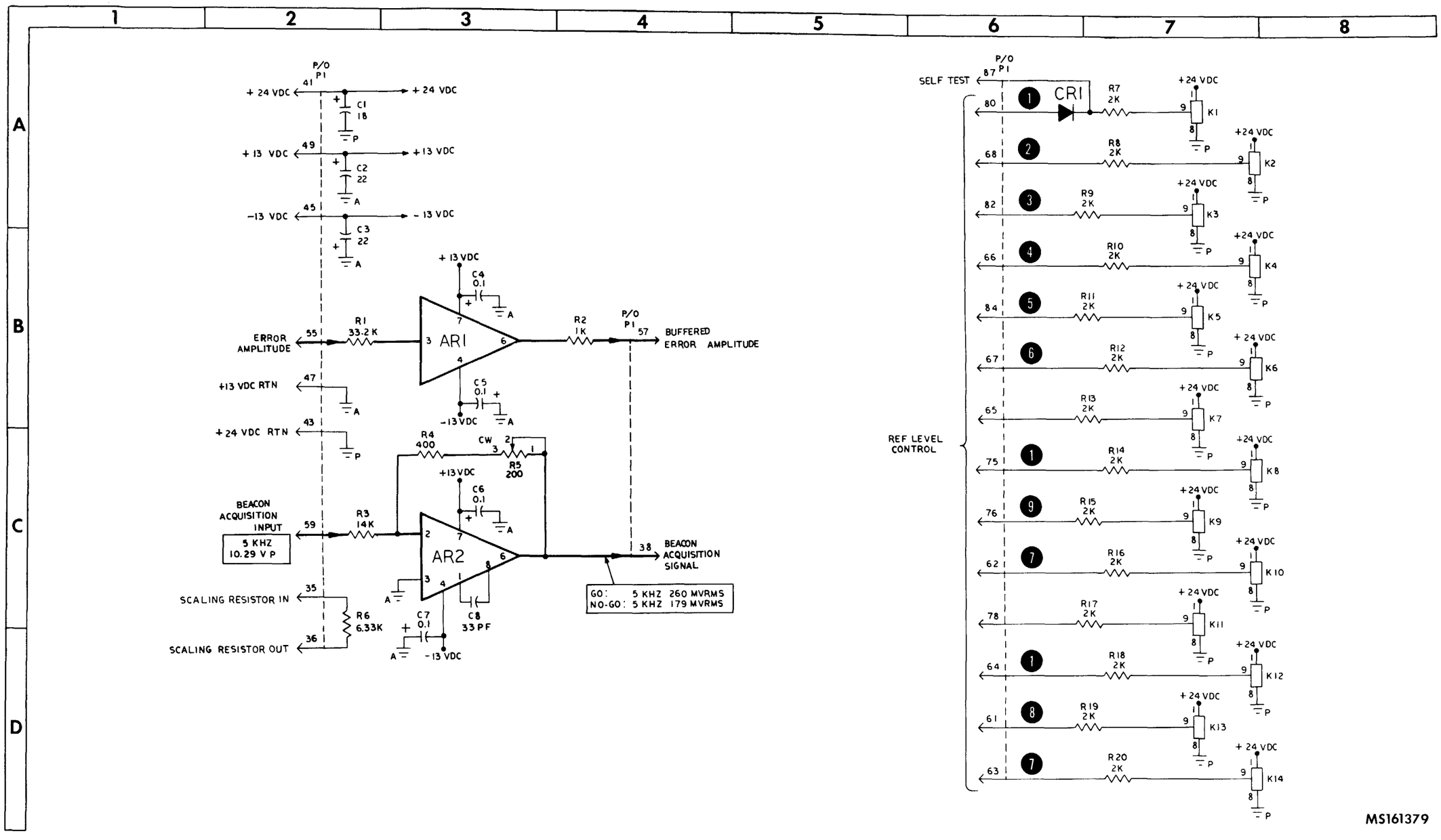


Figure 4-17. DMS-D card A16-schematic diagram (sheet 1 of 5)

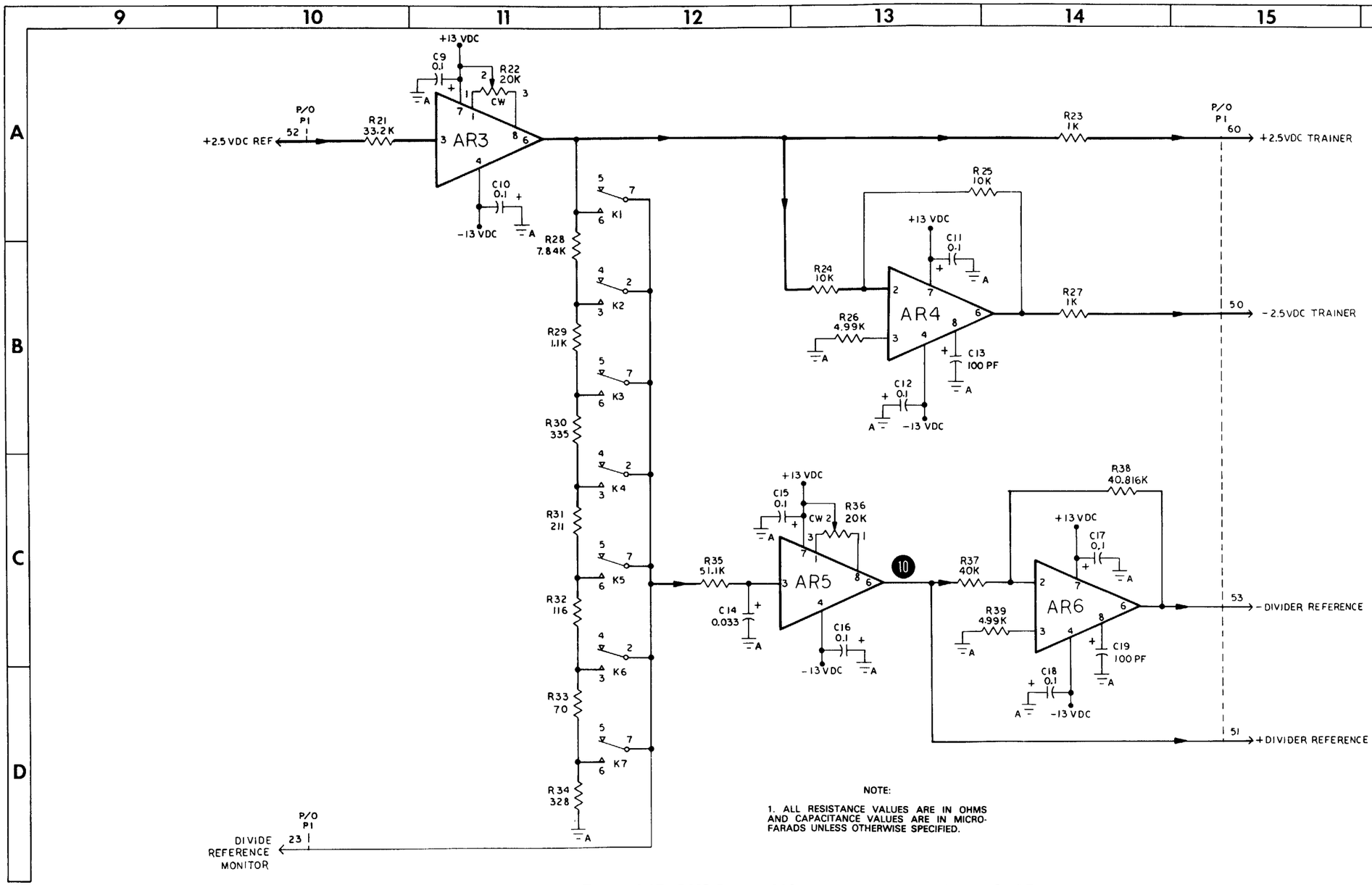


Figure 4-17. DMS-D card A16 schematic diagram (sheet 2 of 5)

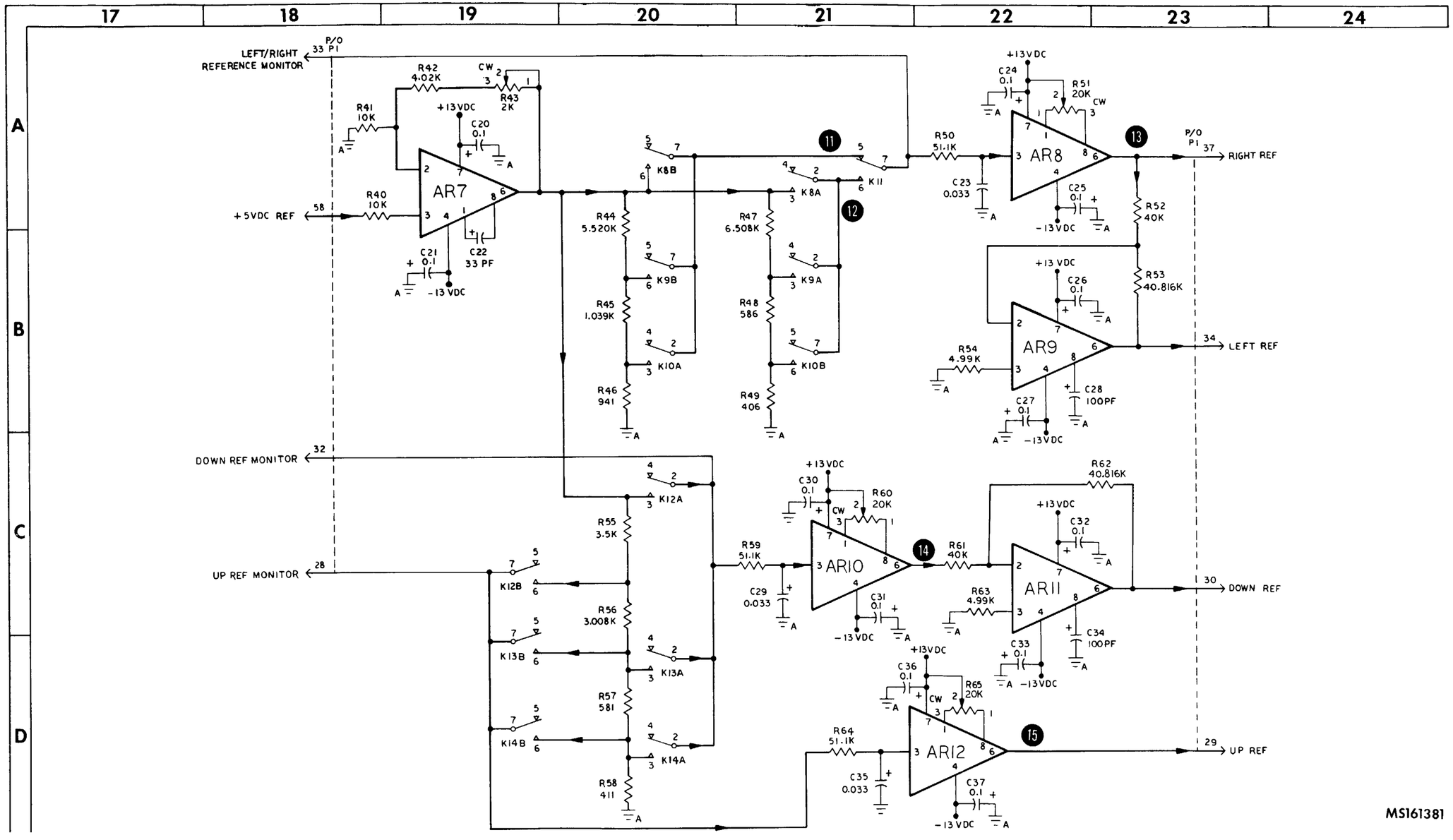
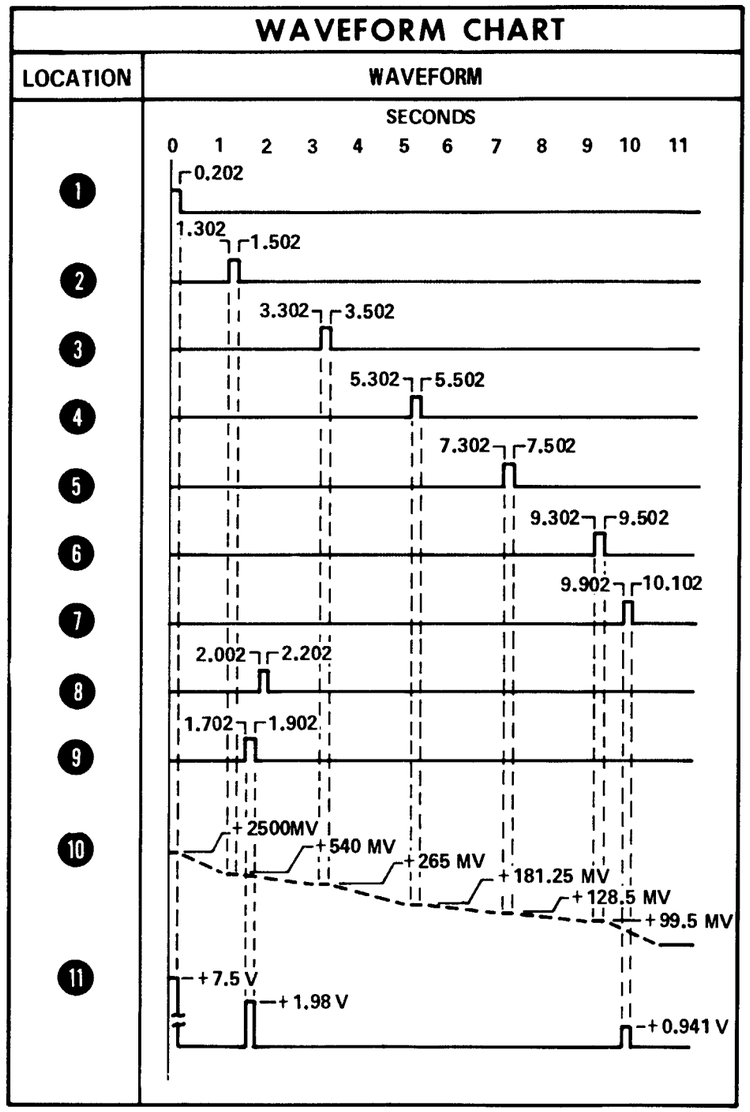


Figure 4-17. DMS-D card A16-schematic diagram (sheet 3 of 5)



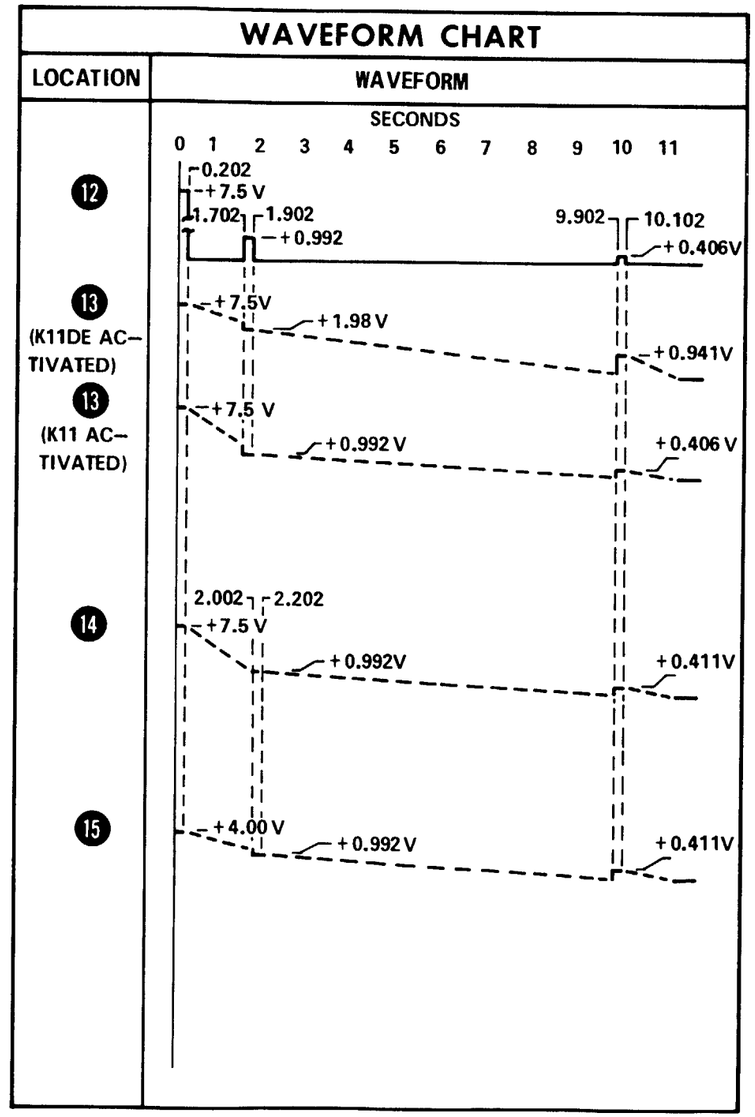


Figure 4-17. DMS-D card A16-schematic diagram (sheet 4 of 5)

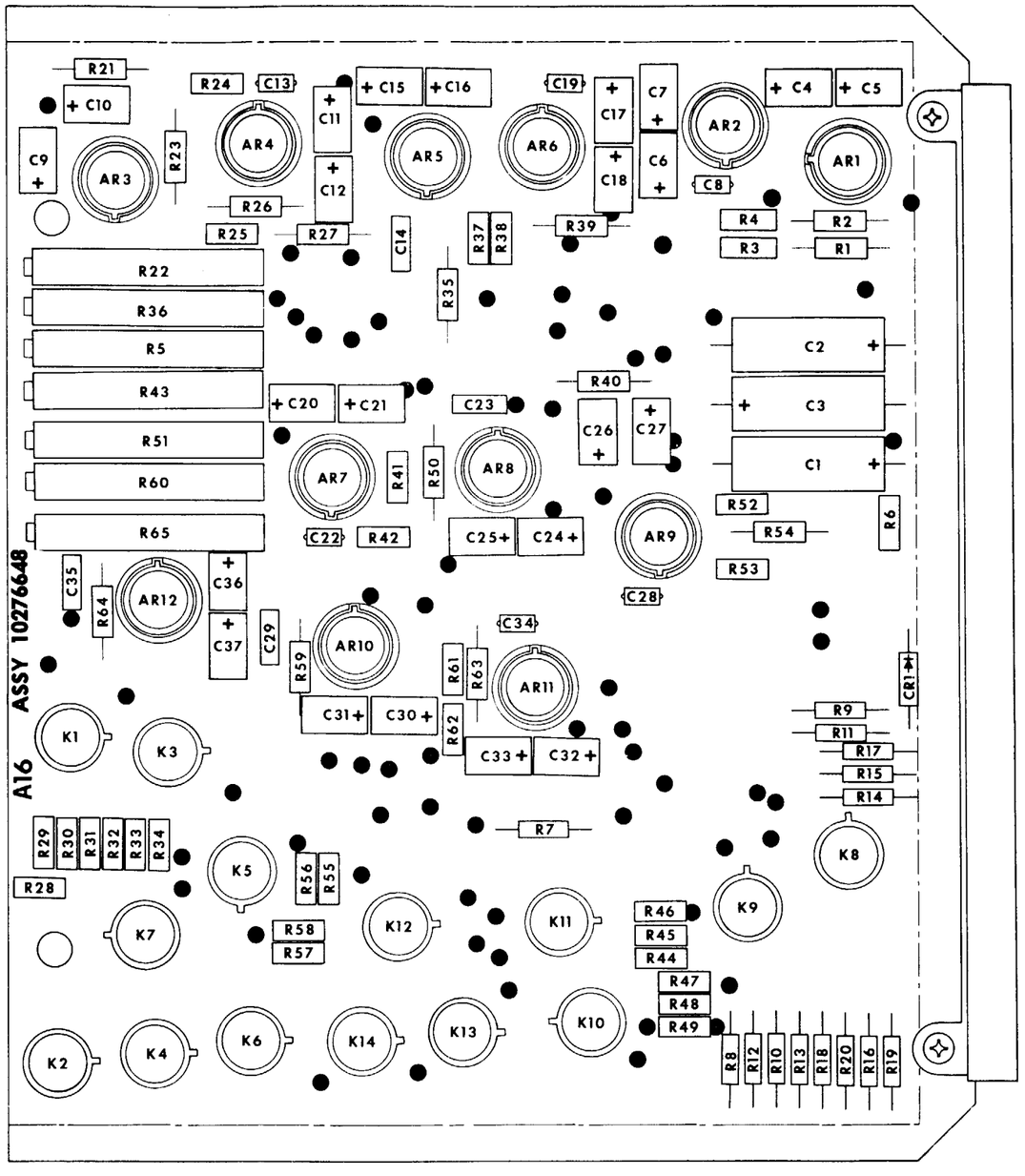


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Figure 4-17. DMS-D card A16-schematic diagram (sheet 5 of 5)

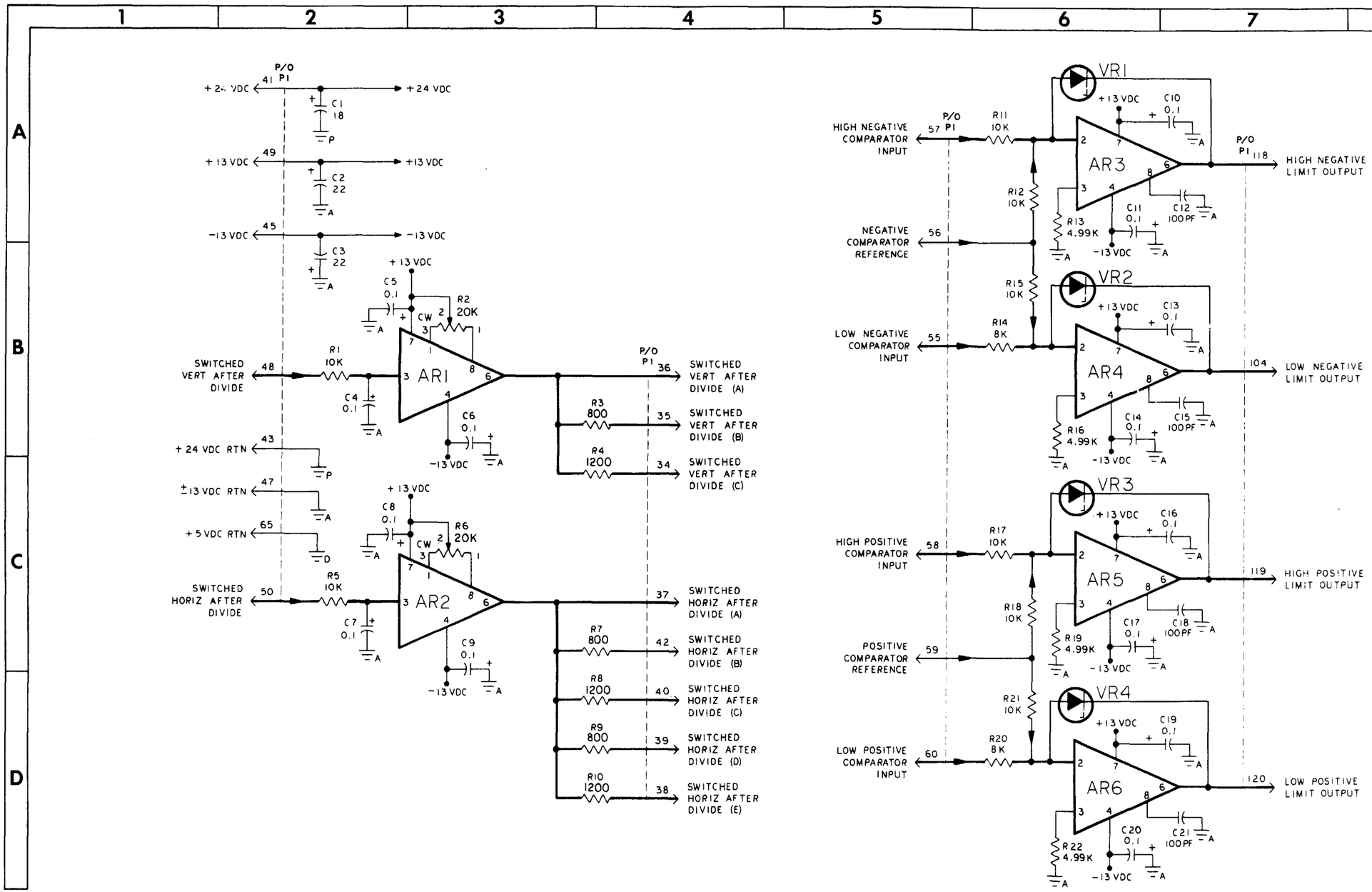


Figure 4-18. DMS-D card A17 (10276474)-schematic diagram (sheet 1 of 4)

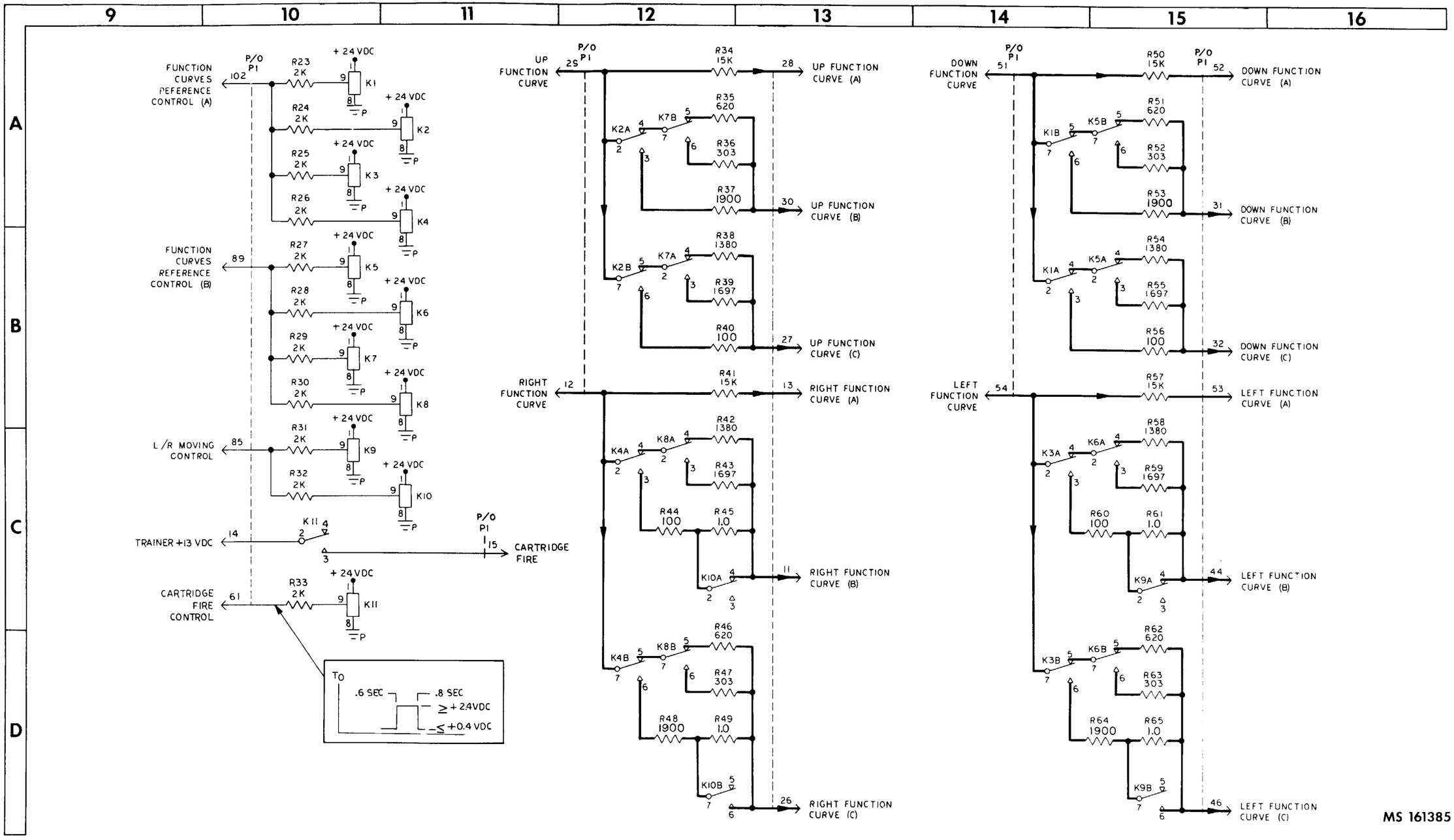


Figure 4-18. DMS-D card A17(10276474) - schematic diagram (sheet 2 of 4)

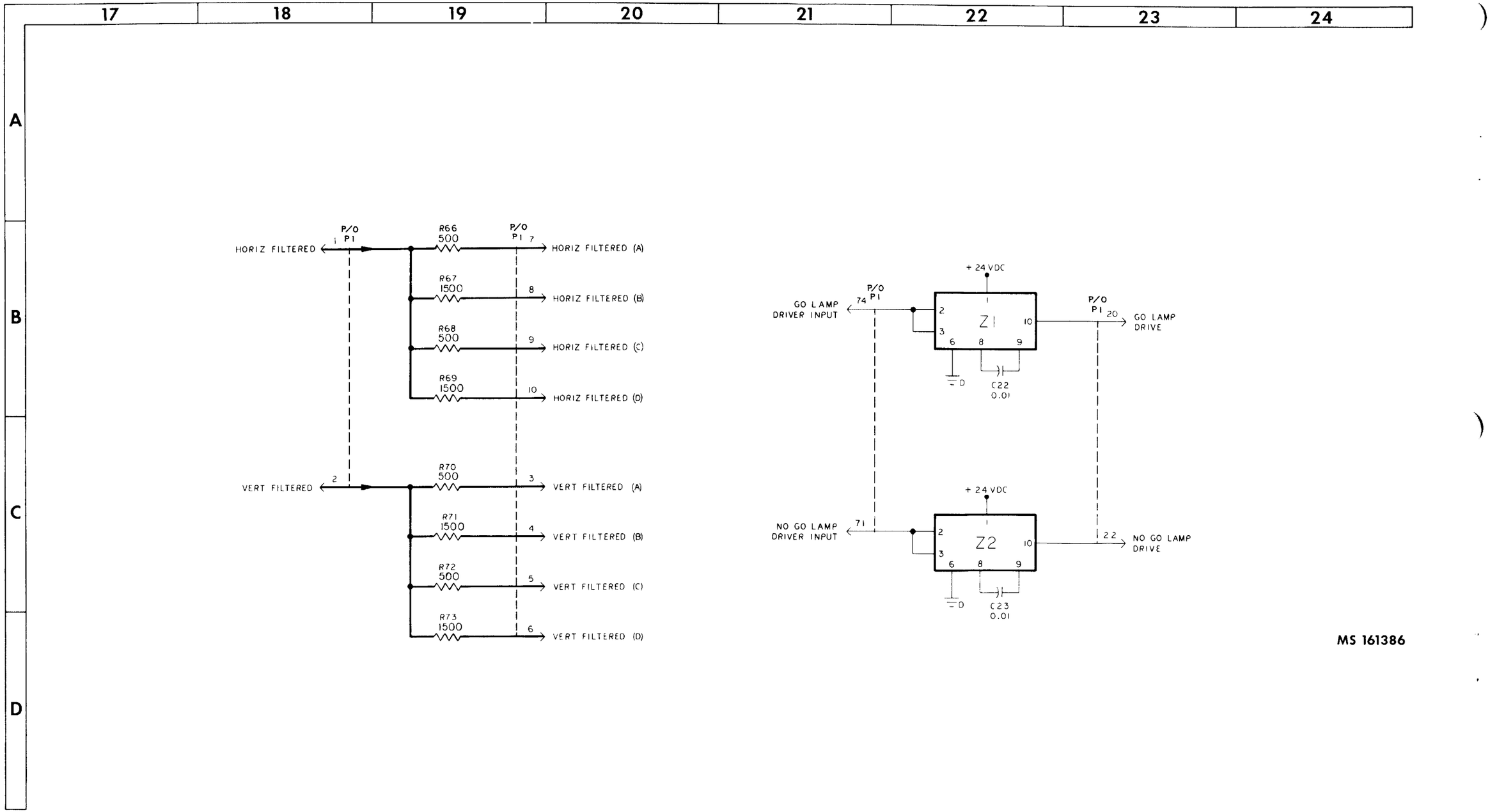


Figure 4-18. DMS-D card A17 (10276474) - schematic diagram (sheet 3 of 4)

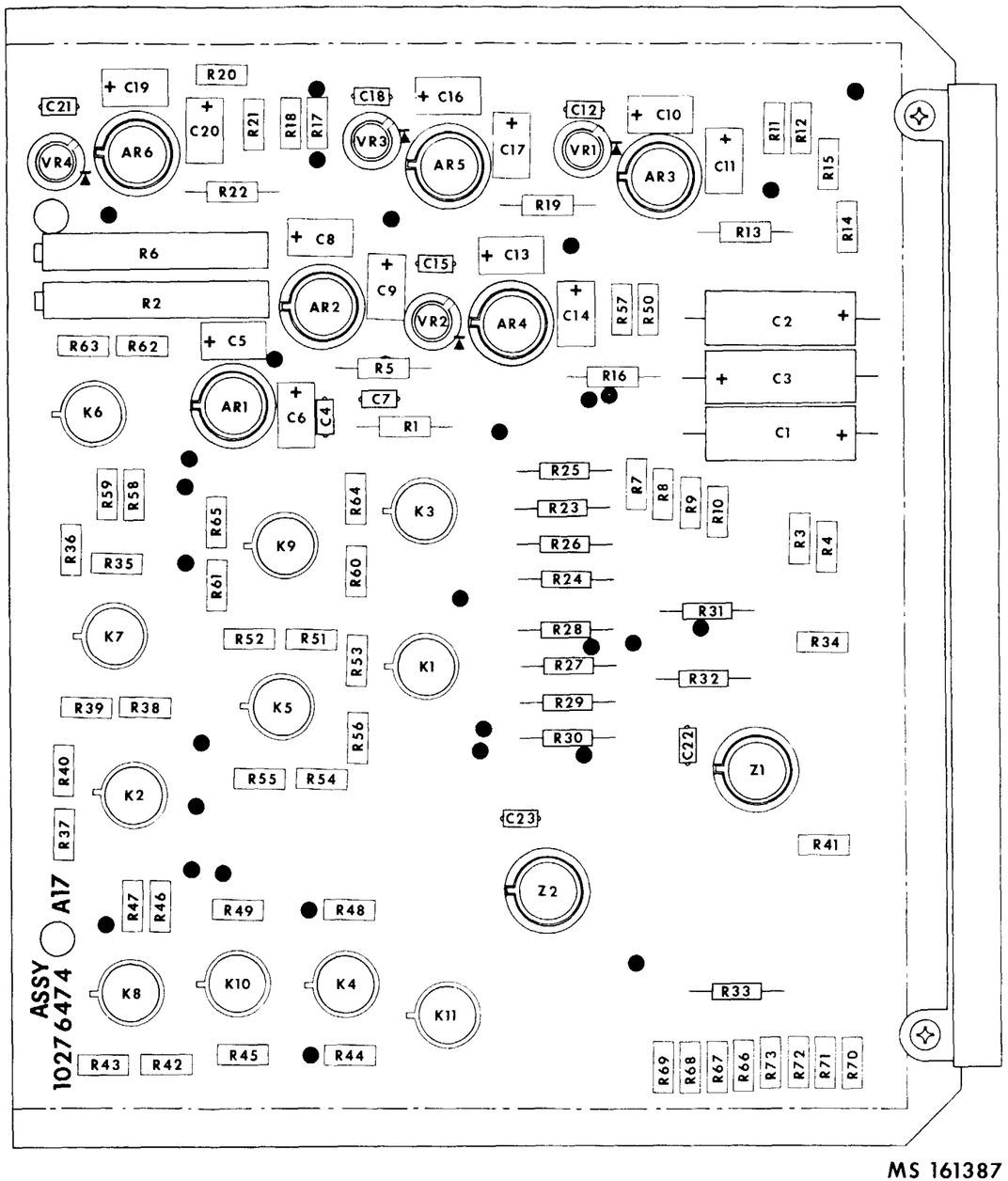
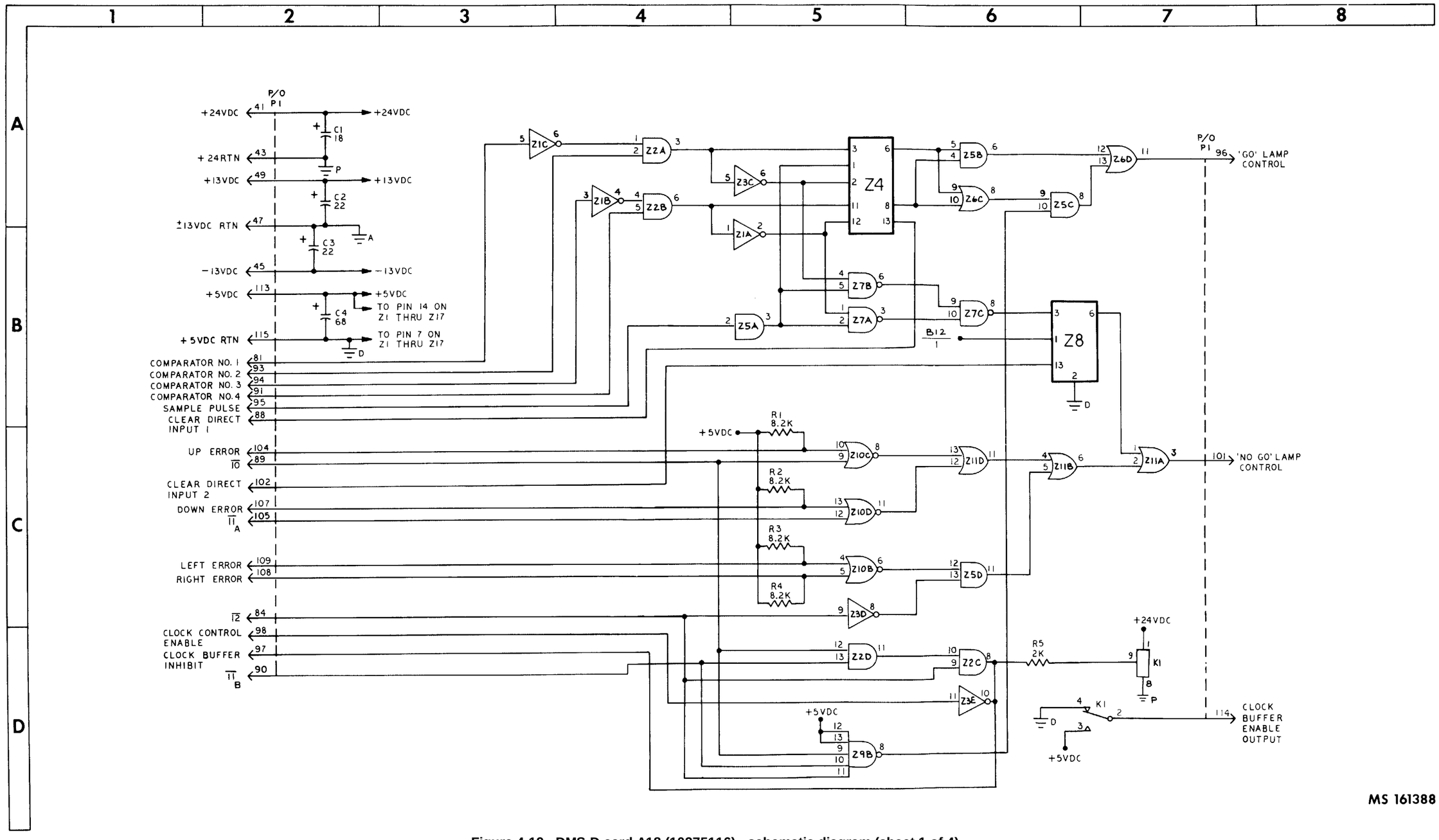
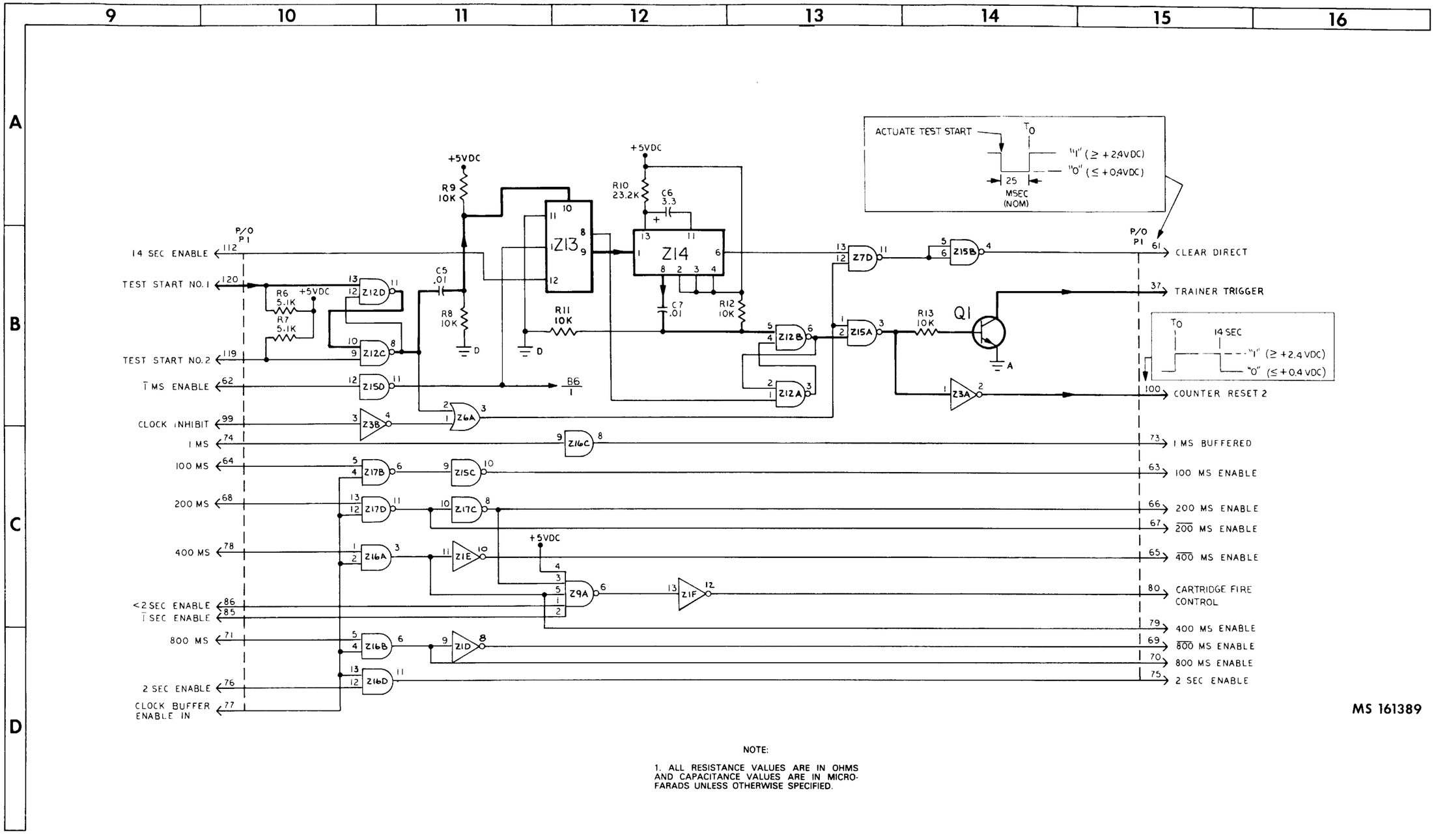


Figure 4-18. DMS-D card A17 - schematic diagram (sheet 4 of 4)



MS 161388

Figure 4-19. DMS-D card A18 (10275116) - schematic diagram (sheet 1 of 4)



MS 161389

NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

Figure 4-19. DMS-D card A18 schematic diagram (sheet 2 of 4)

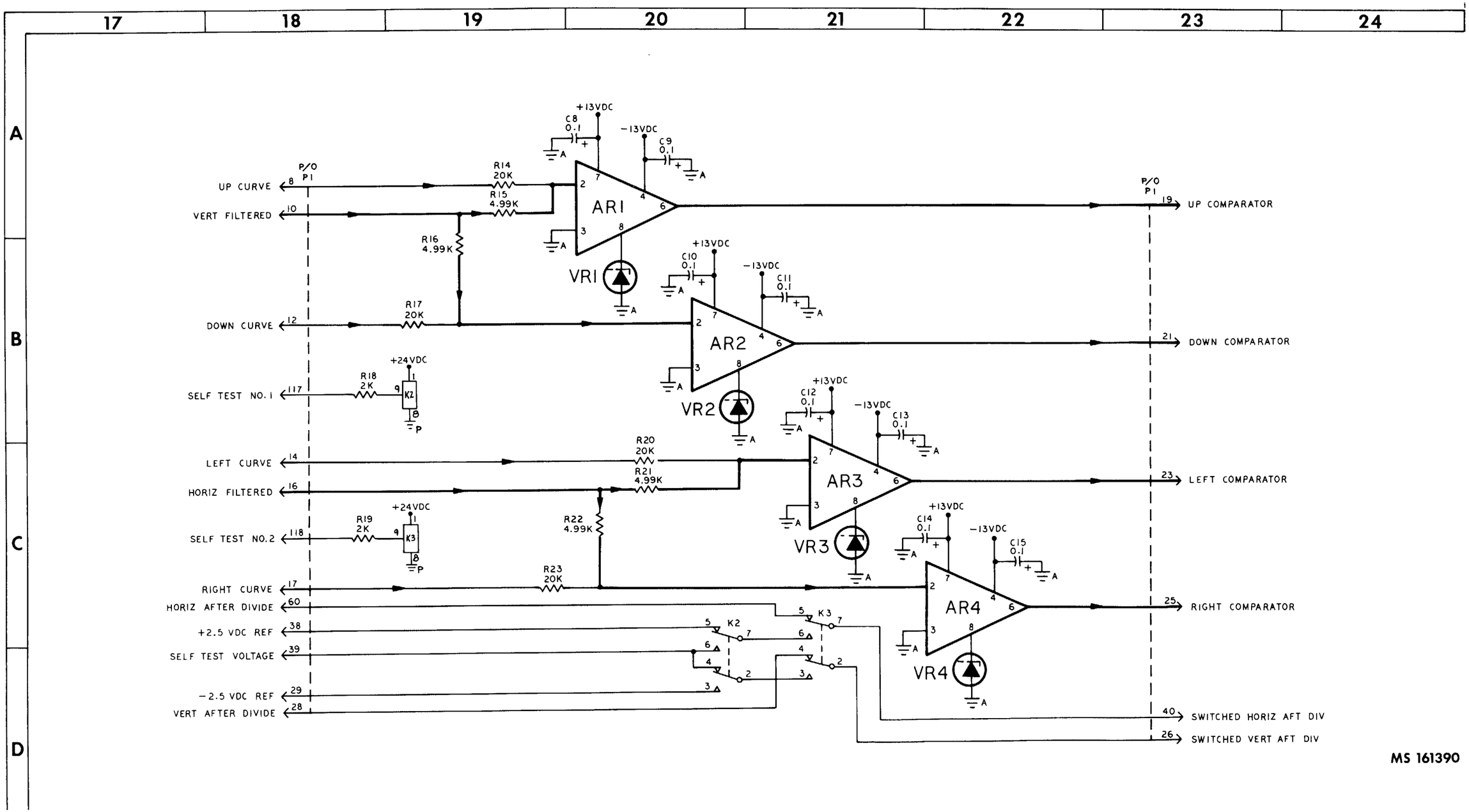


Figure 4-19. DMS-D card A18 (10275116) - schematic diagram (sheet 3 of 4)

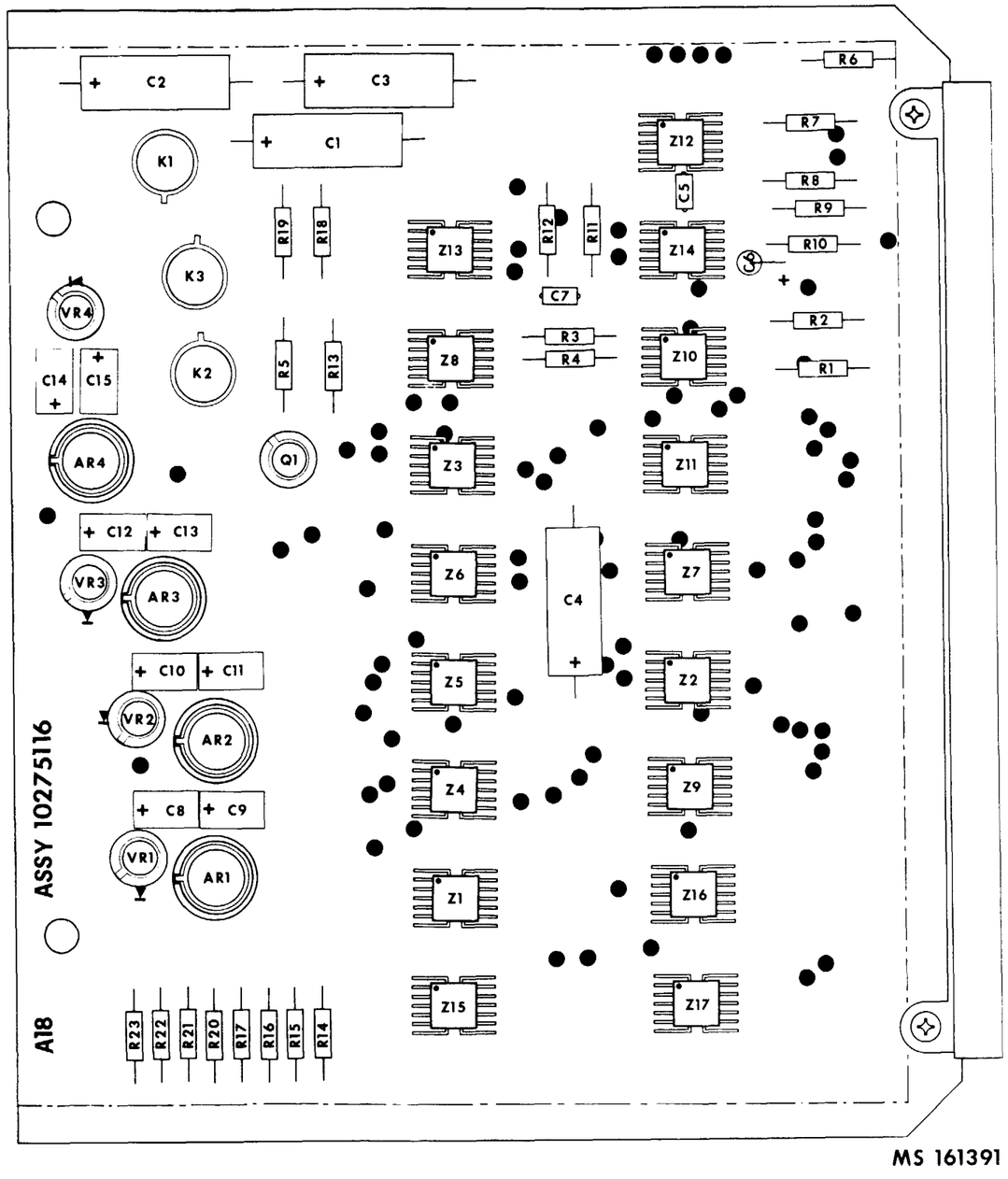
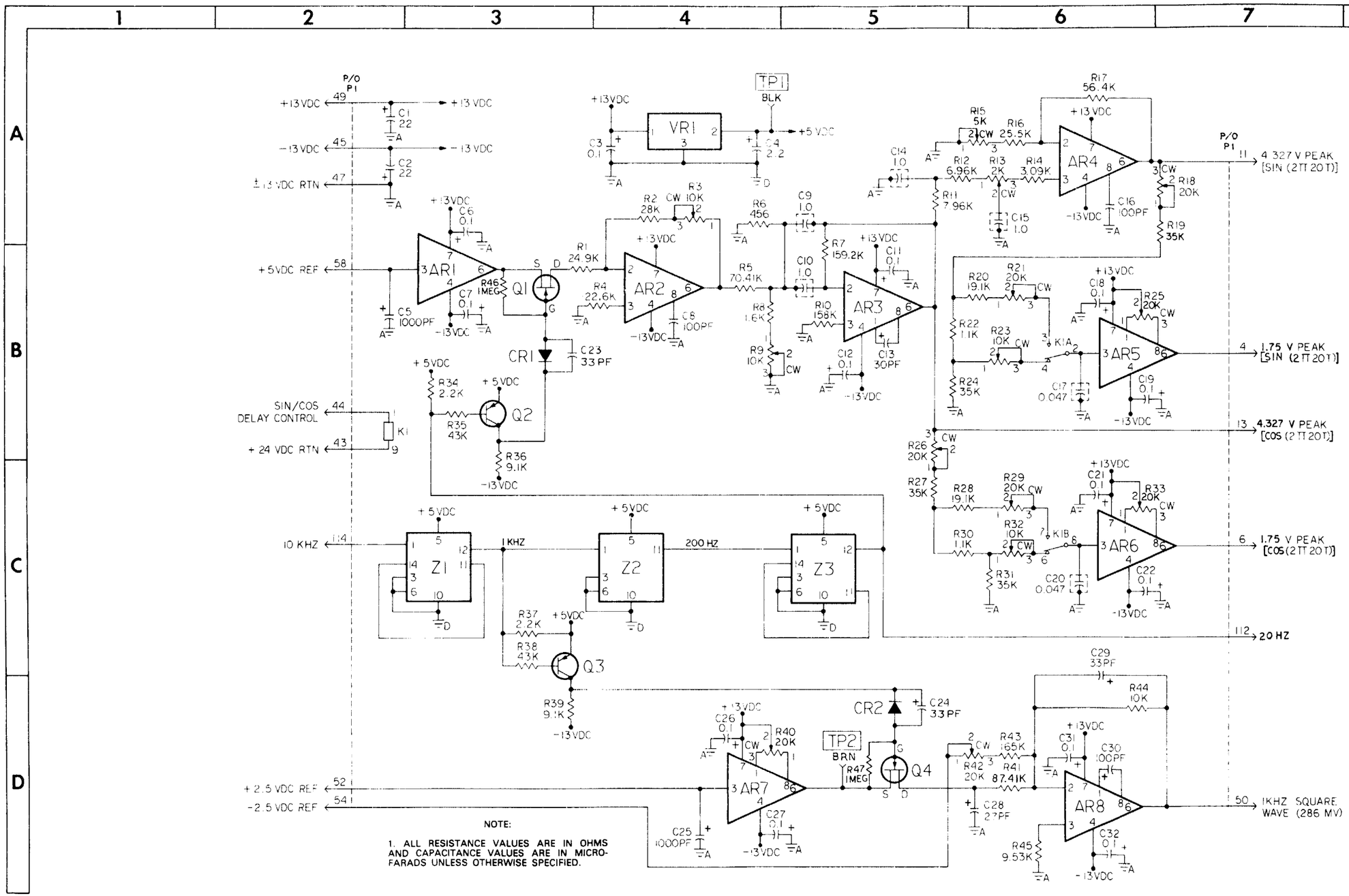


Figure 4-19. DMS-D card A18 (10275116) - schematic diagram (sheet 4 of 4)



MS 161392

Figure 4-20. DMS-D card A19 schematic diagram (sheet 1 of 2)

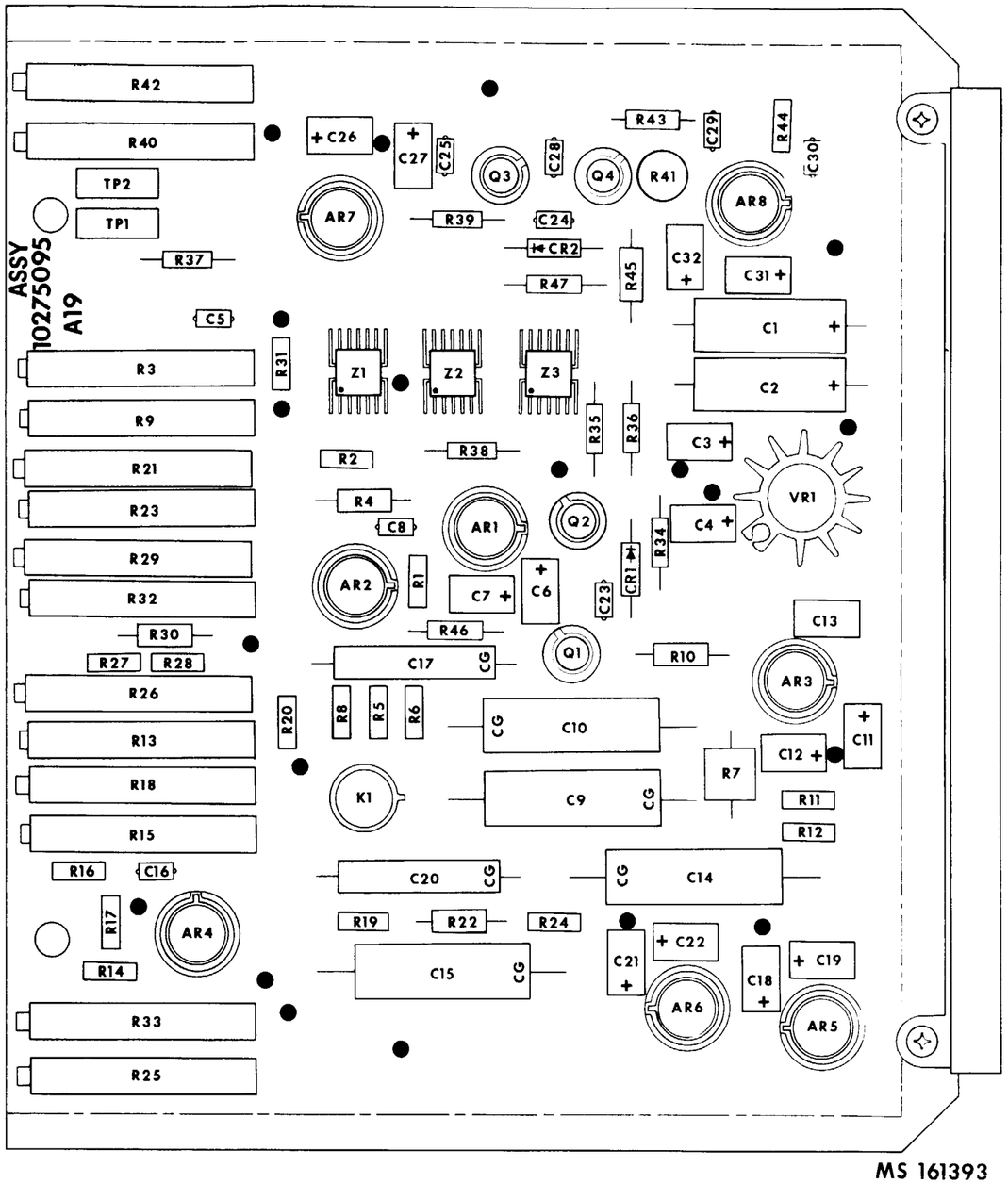
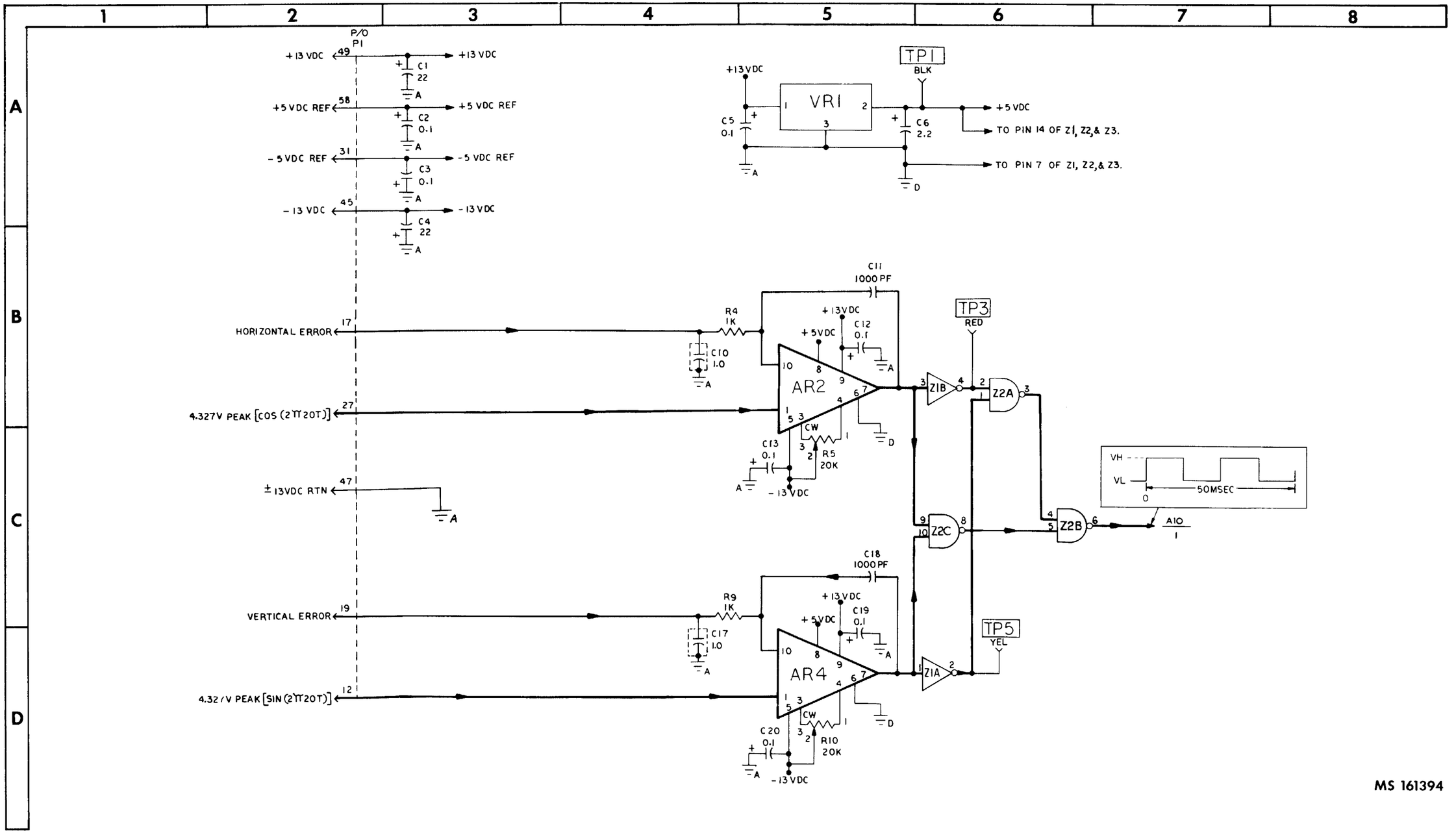
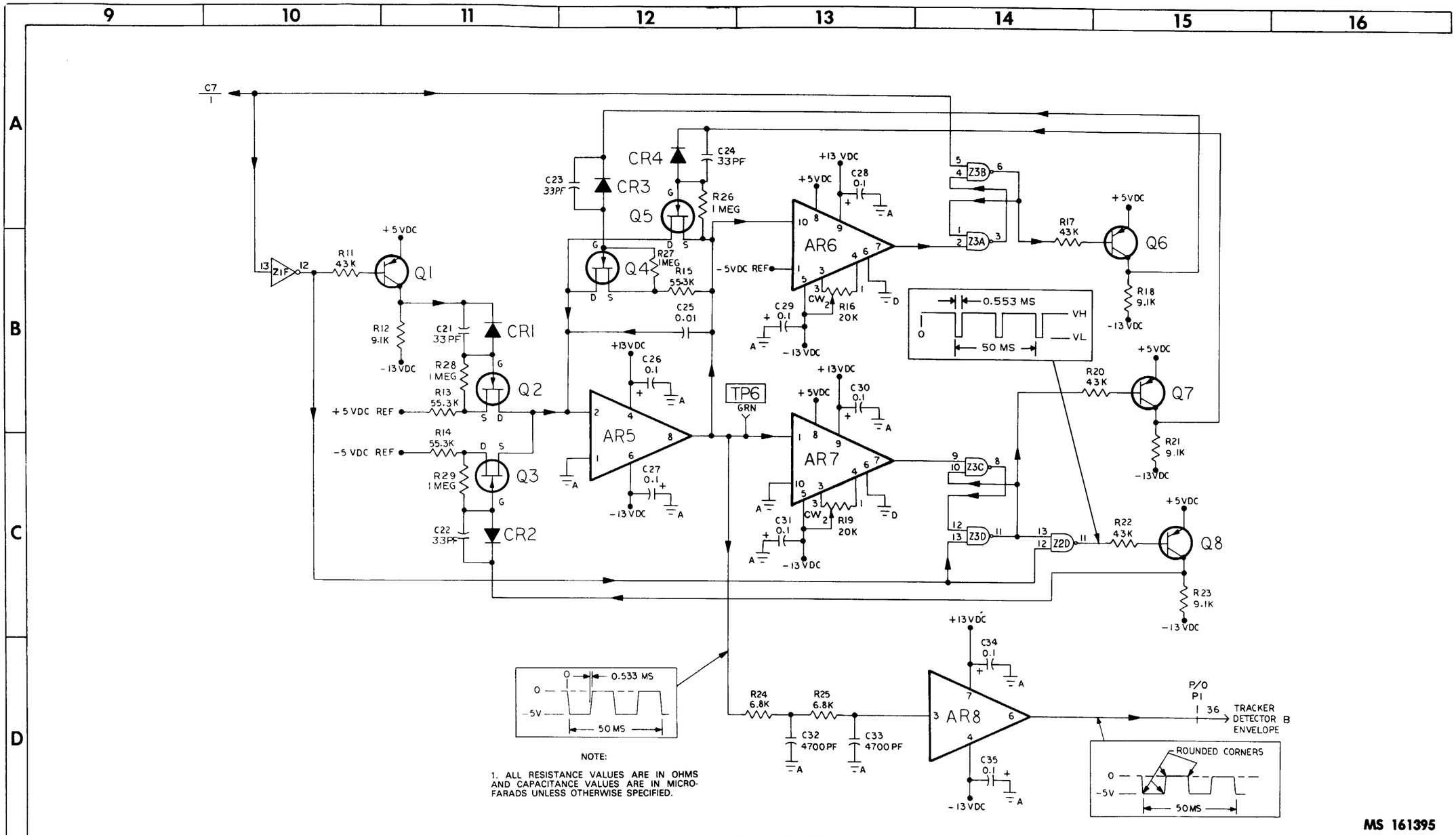


Figure 4-20. DMS-D card A19 schematic diagram (sheet 2 of 2)



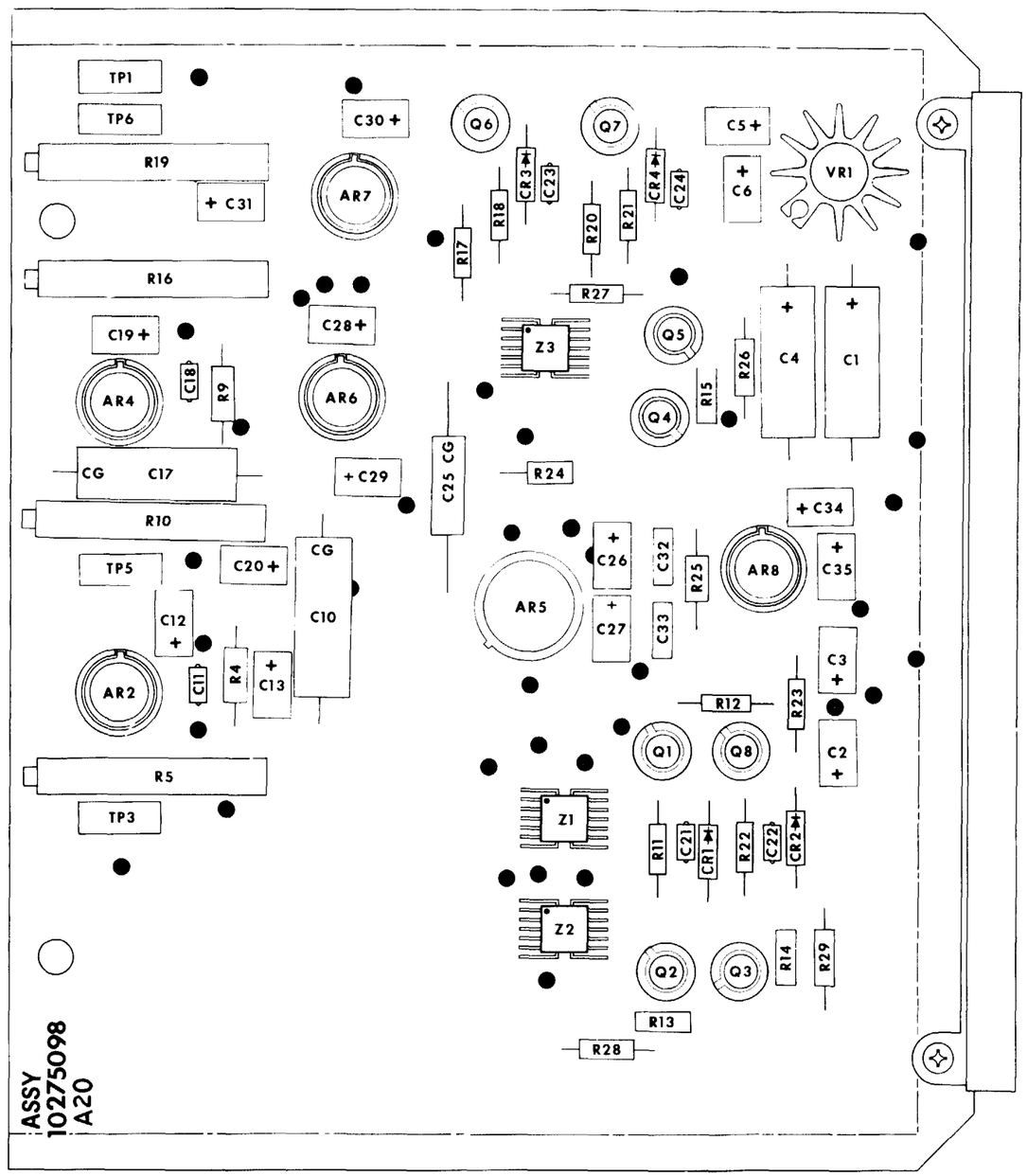
MS 161394

Figure 4-21. DMS-D card A20 (102750981 - schematic diagram (sheet 1 of 3)



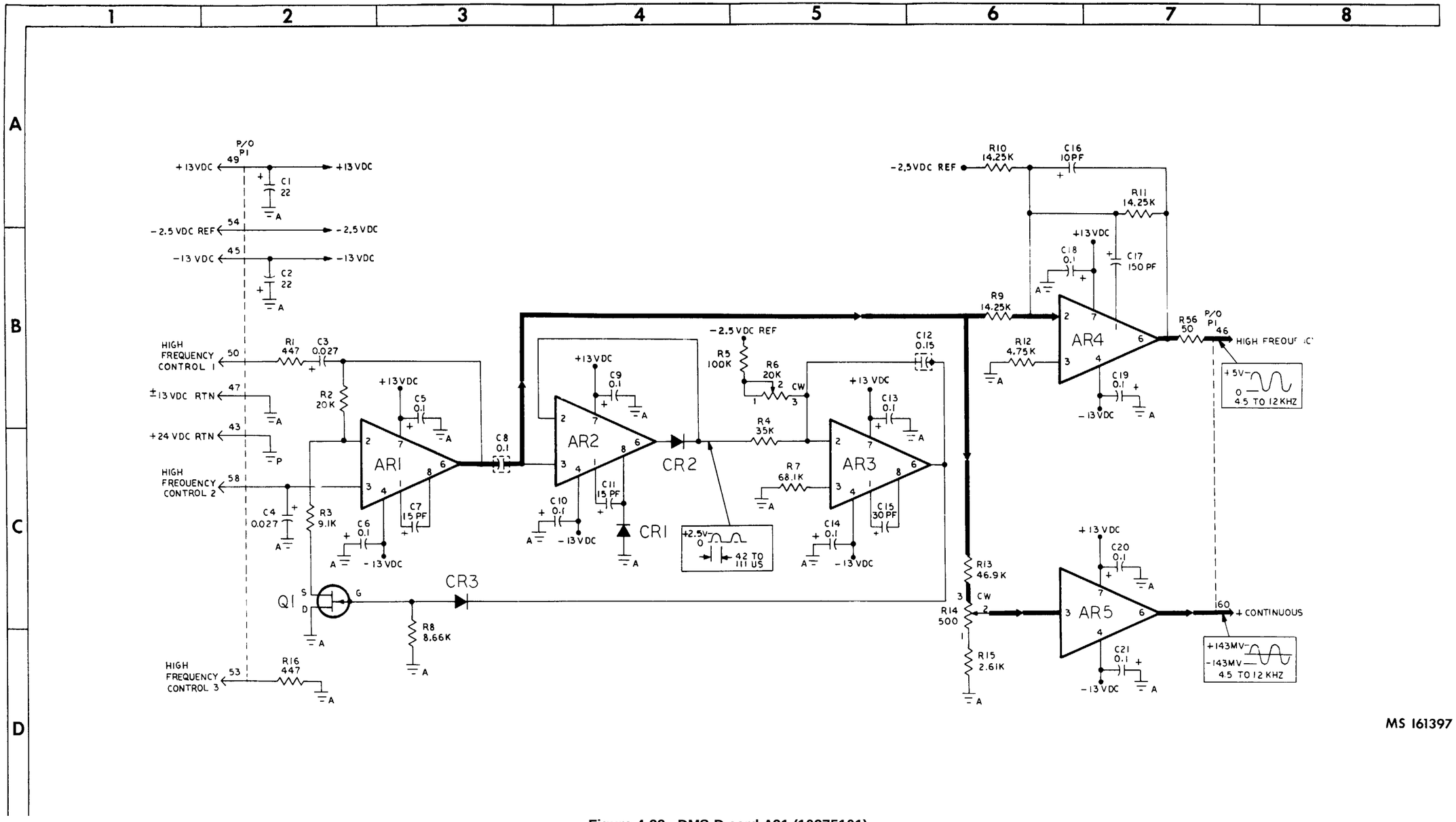
MS 161395

Figure 4-21. DMS-D card A20 schematic diagram (sheet 2 of 3)



MS 161396

Figure 4-21. DMS-D card A20 (10275098)-schematic diagram (sheet 3 of 3)



MS 161397

Figure 4-22. DMS-D card A21 (10275101)-schematic diagram (sheet 1 of 4)

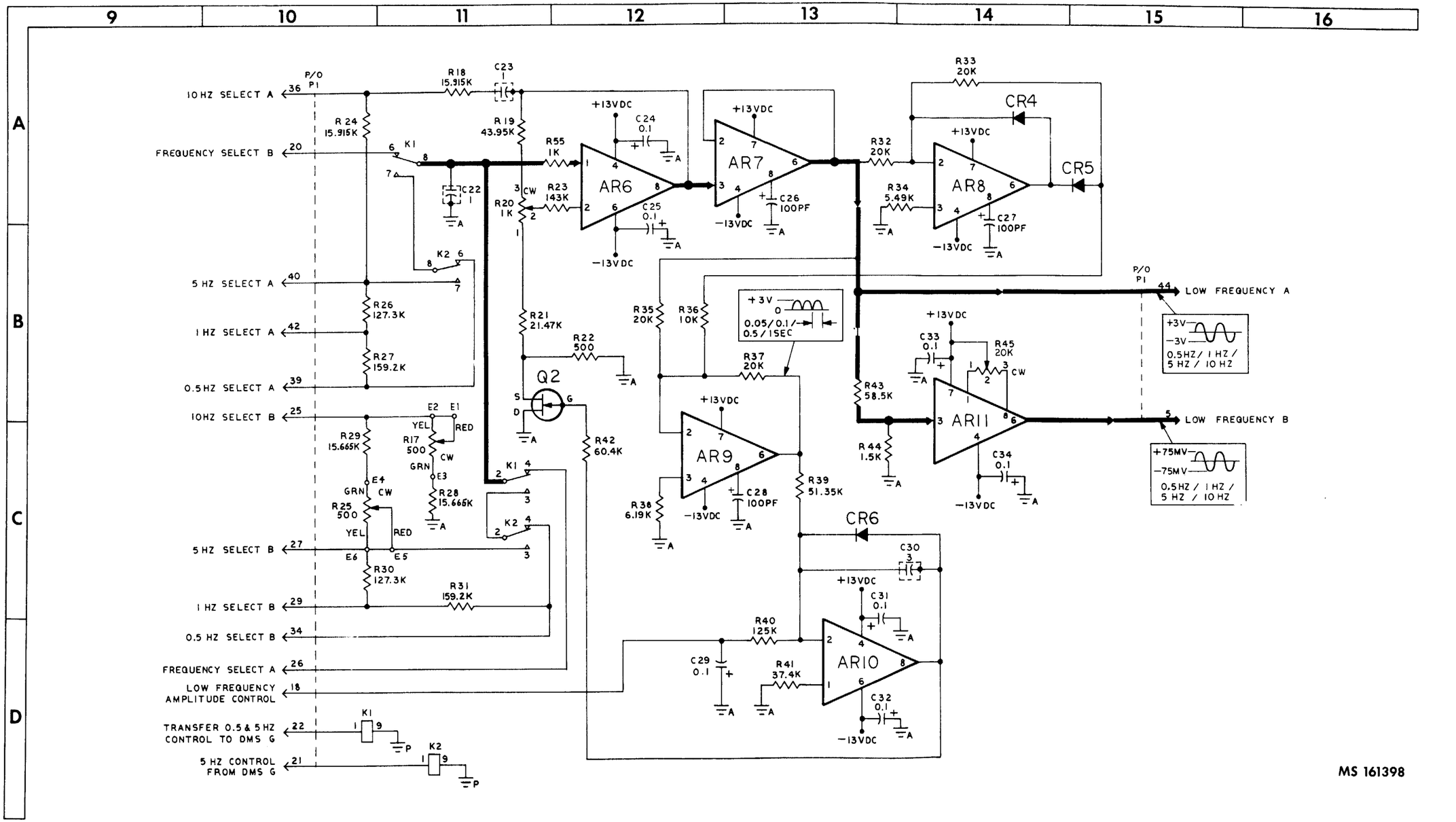


Figure 4-22. DMS-D card A21- schematic diagram(sheet 2 of 4)

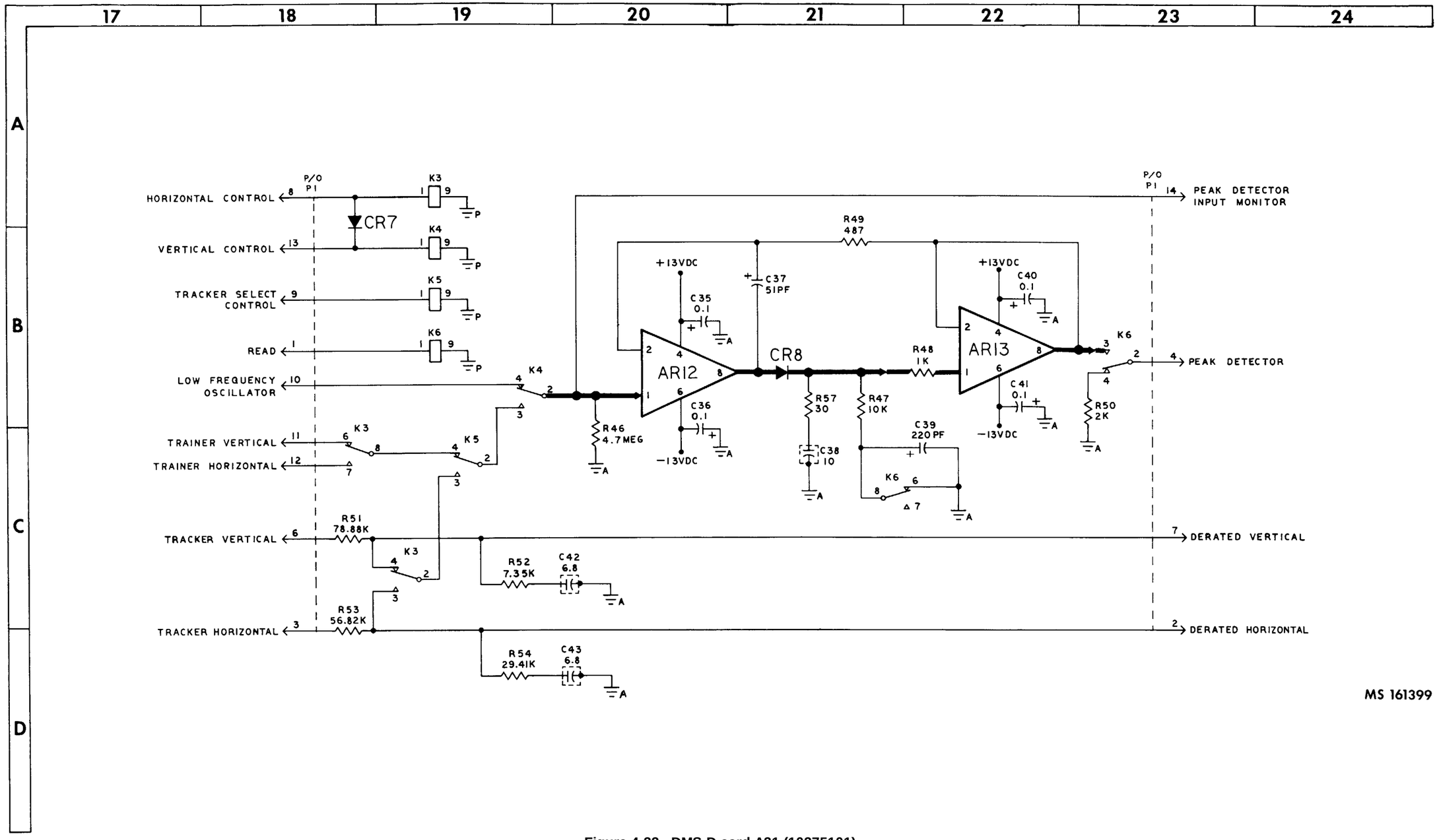
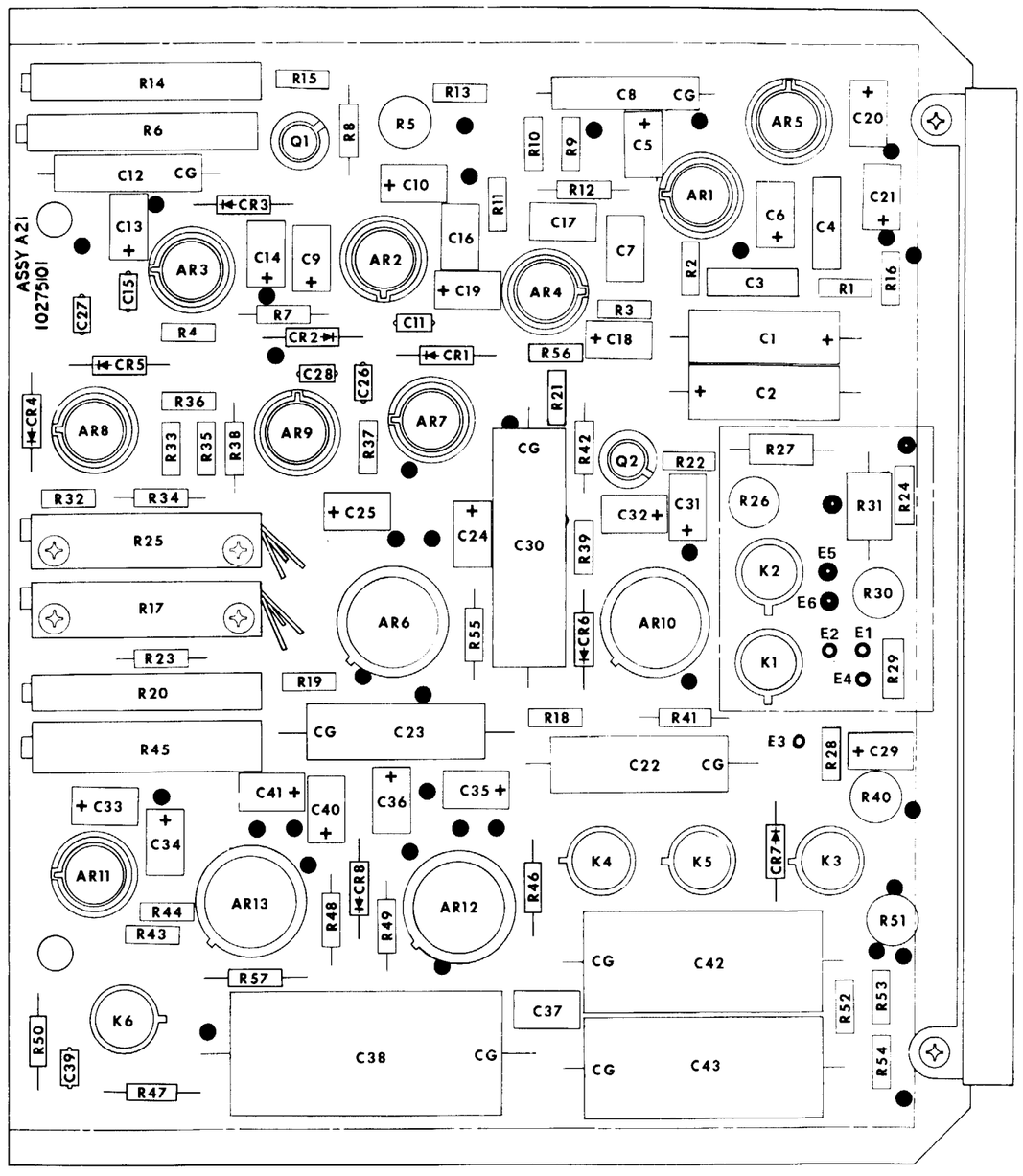
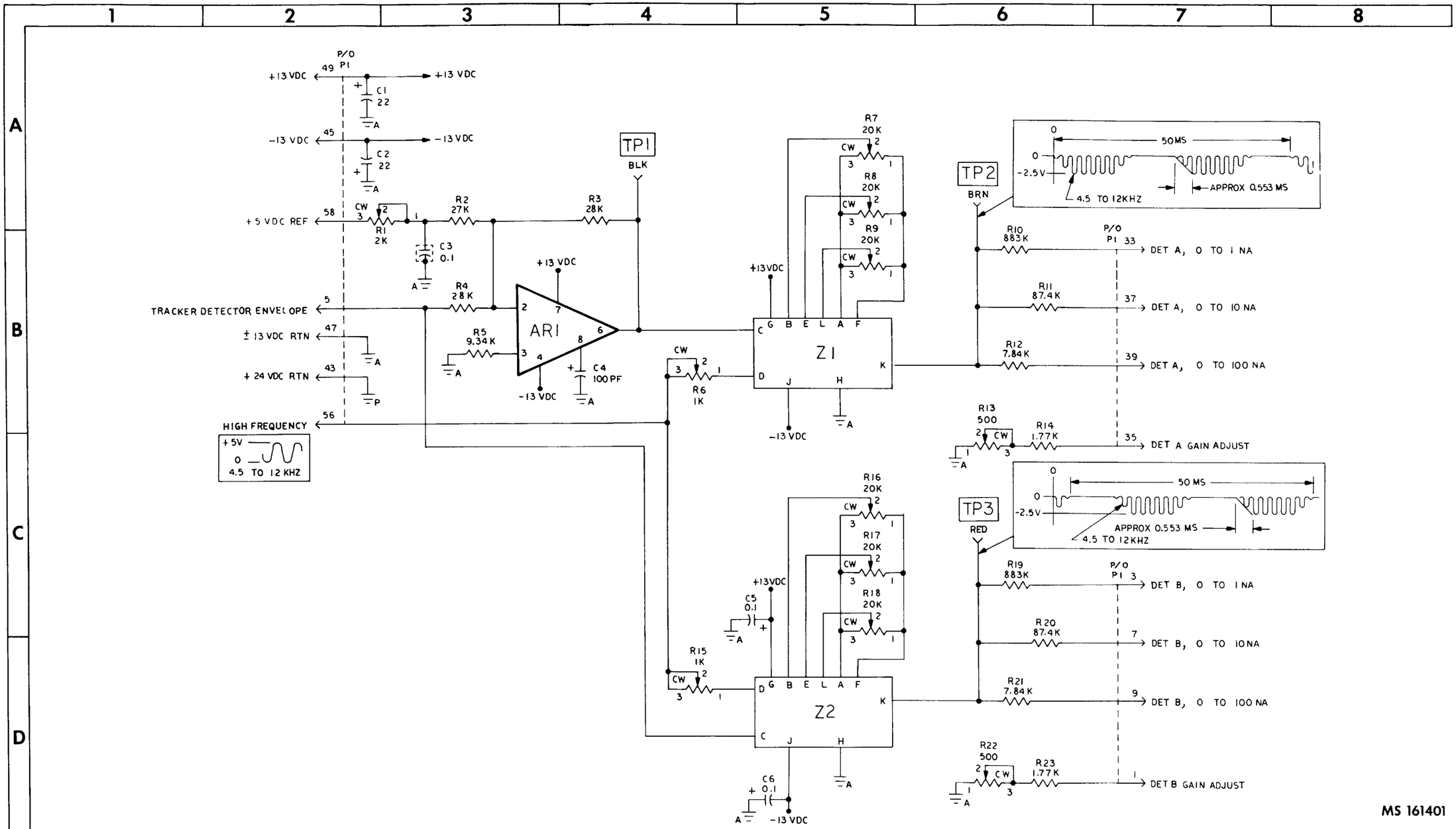


Figure 4-22. DMS-D card A21 (10275101)-schematic diagram (sheet 3 of 4)



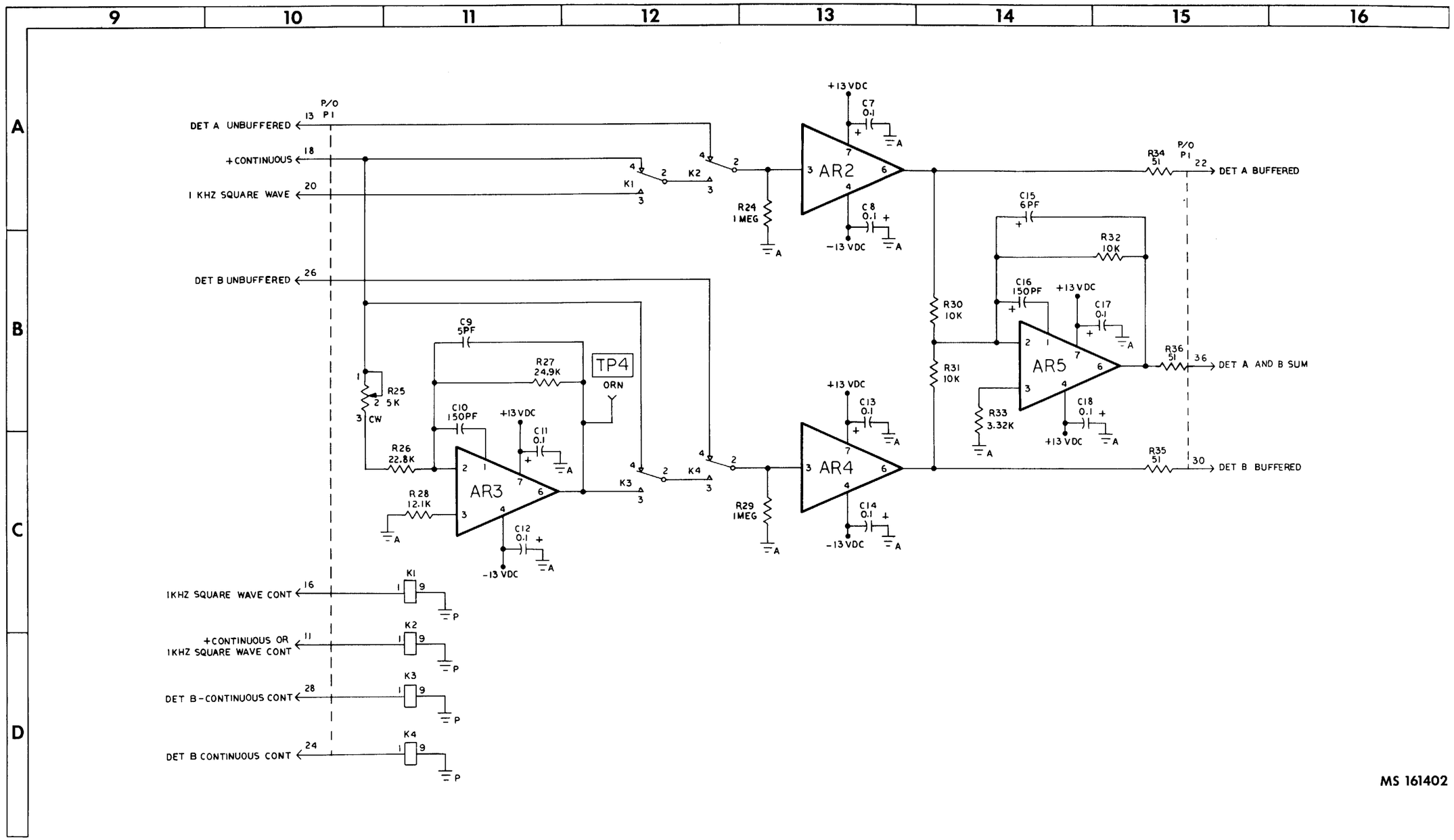
MS 161400

Figure 4-22. DMS-D card A21 schematic diagram (sheet 4 of 4)



MS 161401

Figure 4-23. DMS-D card A22 (10275104)-schematic diagram (sheet 1 of 3)



MS 161402

Figure 4-23. DMS-D card A22 (10275104)-schematic diagram (sheet 2 of 3)

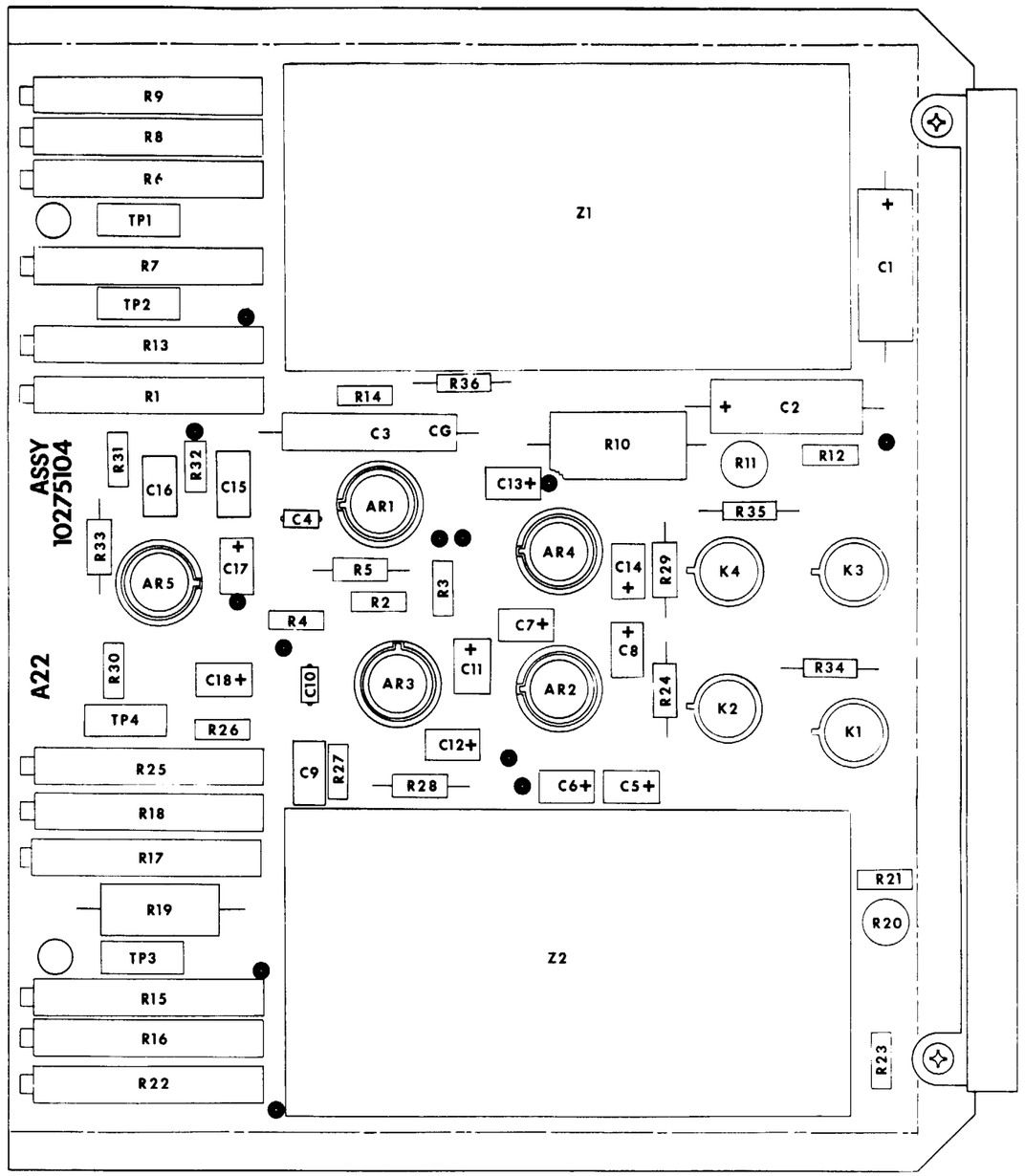


Figure 4-23. DMS-D card A22 (10275104)-schematic diagram (sheet 3 of 3)

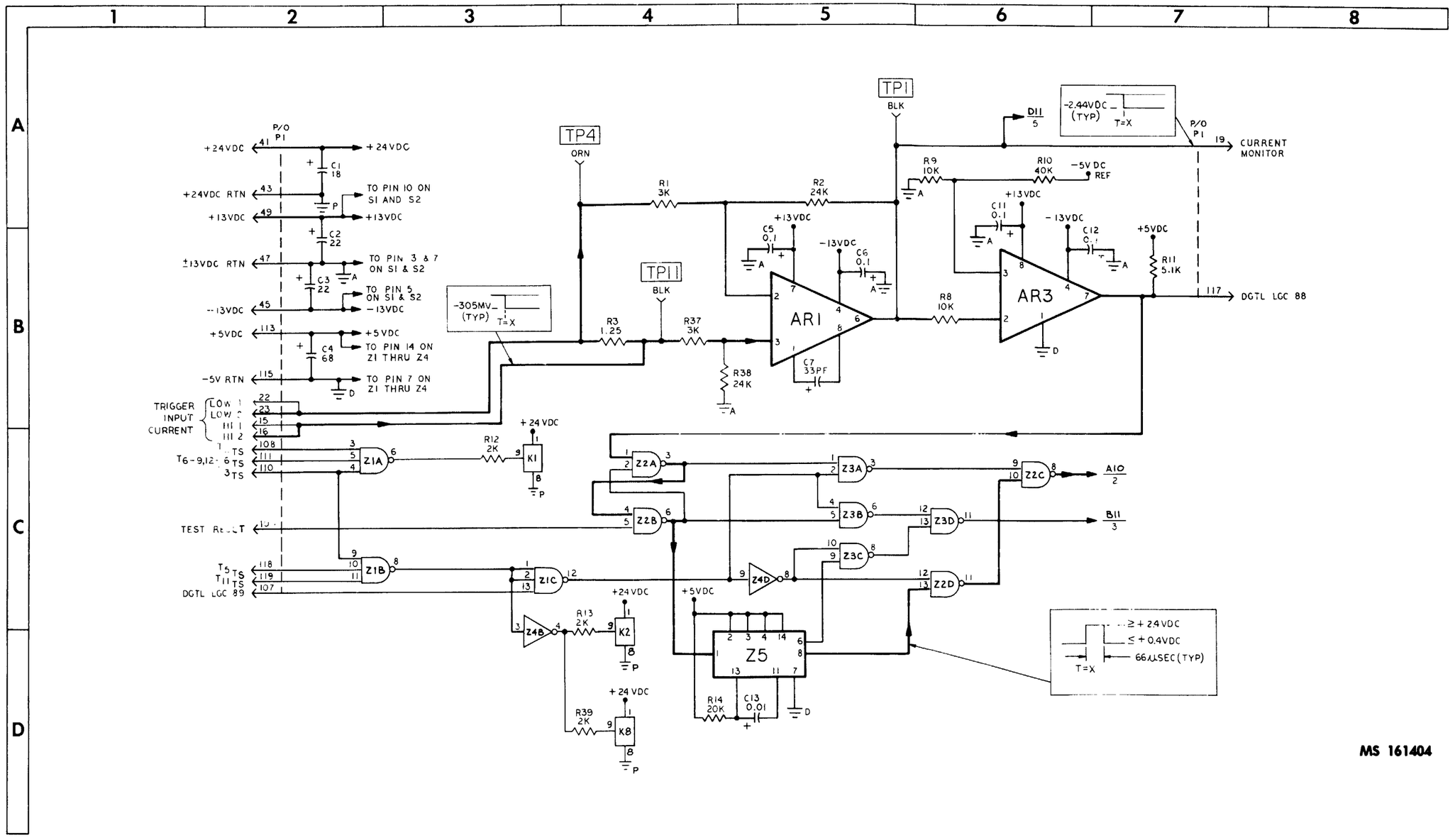
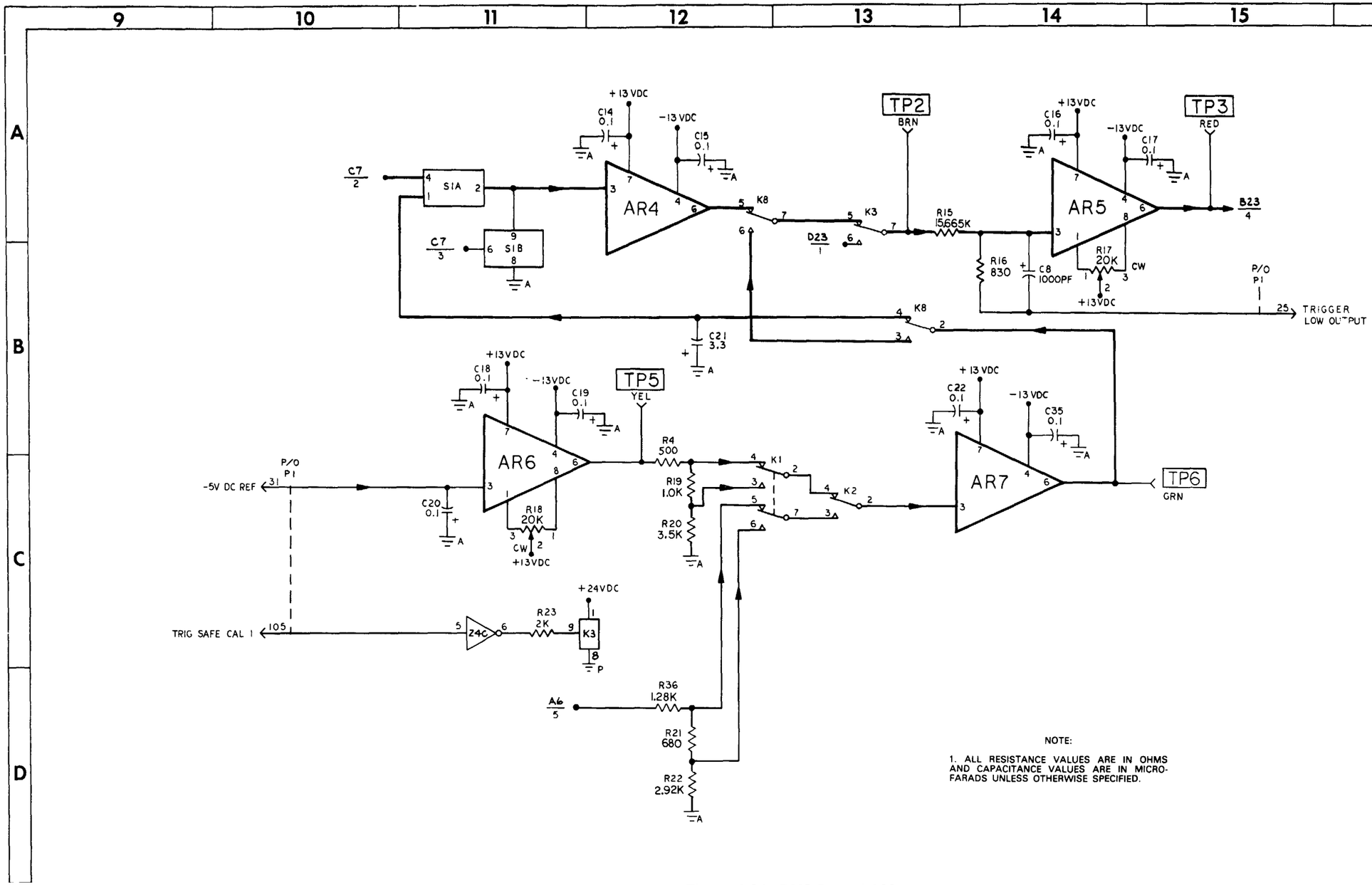


Figure 4-24. DMS-D Card A23 Schematic Diagram (sheet 1 of 5)



MS 161405

Figure 4-24. DMS-D card A23 schematic diagram (sheet 2 of 5)

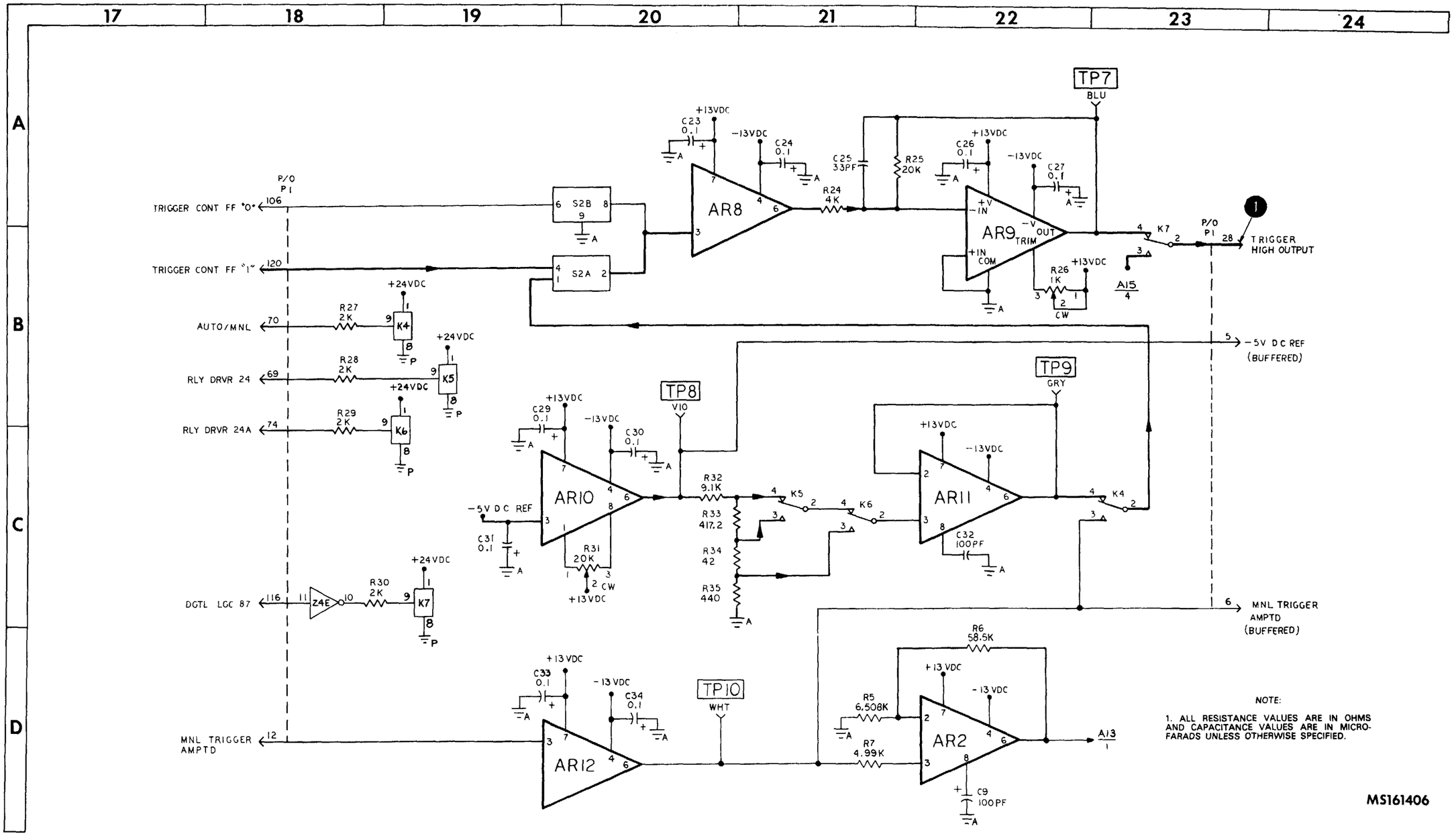


Figure 4-24. DMS-D card A23 schematic diagram (sheet 3 of 5)

WAVEFORM CHART

WAVEFORM LOCATION FOR ❶	
INPUT FROM TRACKER TEST SET (TTS)	0 MA — −244 MA (NOM) INTO 1.25 OHM
TRIGGER OUTPUT SWITCH OFF	WAVEFORMS LOCATION FOR ❷
SEQUENCE SWITCH POSITION	
NO. 1	0 V — AMPLITUDE DIRECTLY PROPORTIONAL TO TTS CURRENT — -90 MV (NOM)
NO. 2	0 V — AMPLITUDE DIRECTLY PROPORTIONAL TO TTS CURRENT — -73 MV (NOM)
NO. 3	0 V — 66 µS (NOM) — -175 MV
NO. 4	SAME AS NO. 1
NO. 5	0 V — 66 µS (NOM) — -225 MV
NO. 6–9	SAME AS NO. 2
NO. 10	SAME AS NO. 1
NO. 11	SAME AS NO. 5
NO. 12–16	SAME AS NO. 2
MNL	VARIABLE, 0 TO −500 MVDC CONTROLLED BY TRIGGER PULSE AMPLITUDE POTENTIOMETER.

WAVEFORM CHART

TRIGGER OUTPUT SWITCH POSITION	WAVEFORMS LOCATION FOR ❷
GO TEST	ACTUATE TRIGGER SWITCH — 0 V — +1.205 VDC — 10 MSEC
NO–GO TEST NO. 1	0 V — +2.248 VDC — 2.5 MSEC
NO–GO TEST NO. 2	0 V — +1.100 VDC — 12 MSEC
MNL	2.0 –13.9 MSEC — 0–5 VDC PULSE WIDTH: 2.0 TO 13.9 MILLISECONDS IN 1 INCREMENTS CONTROLLED BY WIDTH (MS) SWITCH. AMPLITUDE: 0 TO +5 VDC CONTROLLED BY AMPTD (VOLTS) POTENTIOMETER.

MS 161407

Figure 4-24. DMS-D card A23 schematic diagram (sheet 4 of 5)

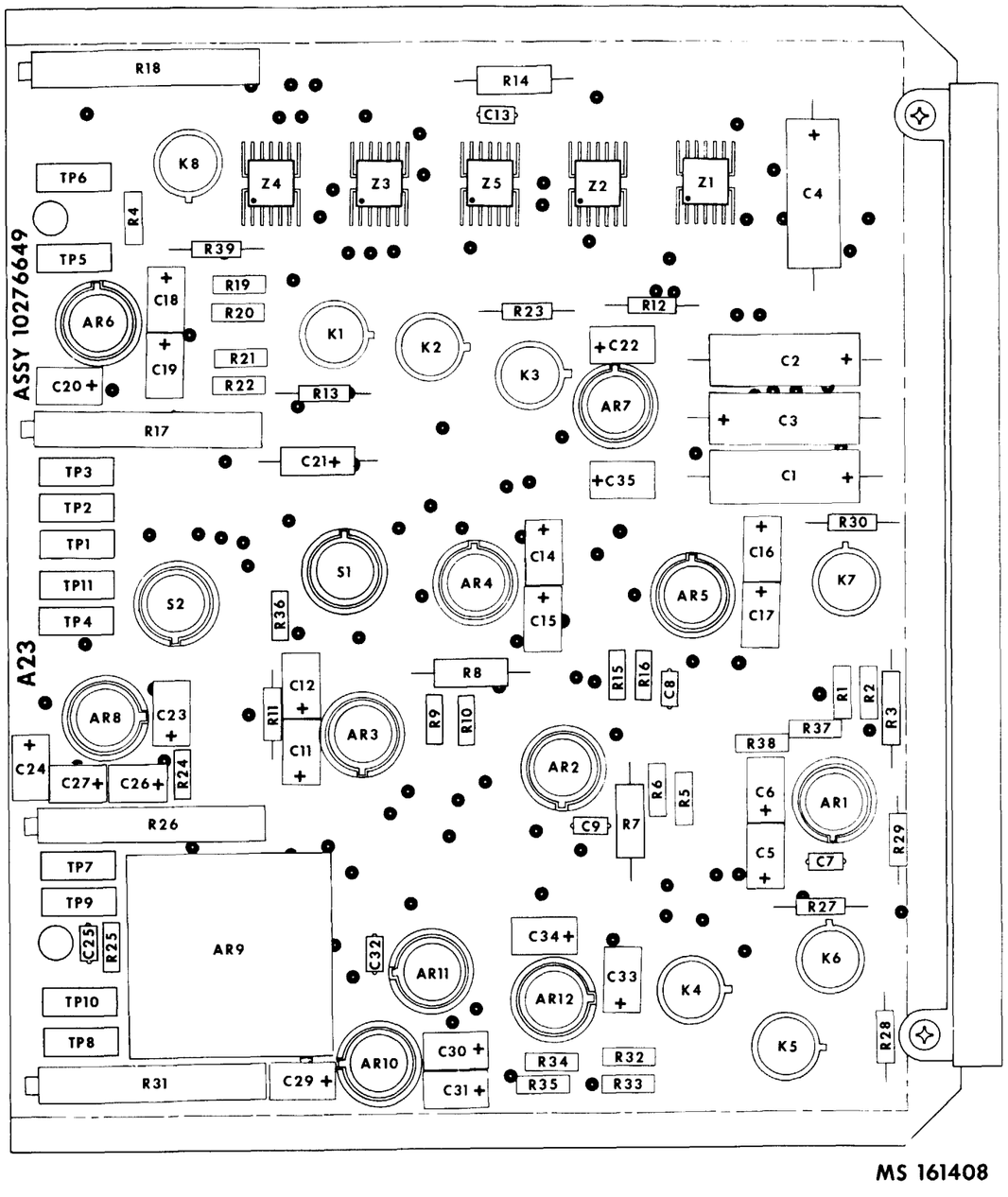
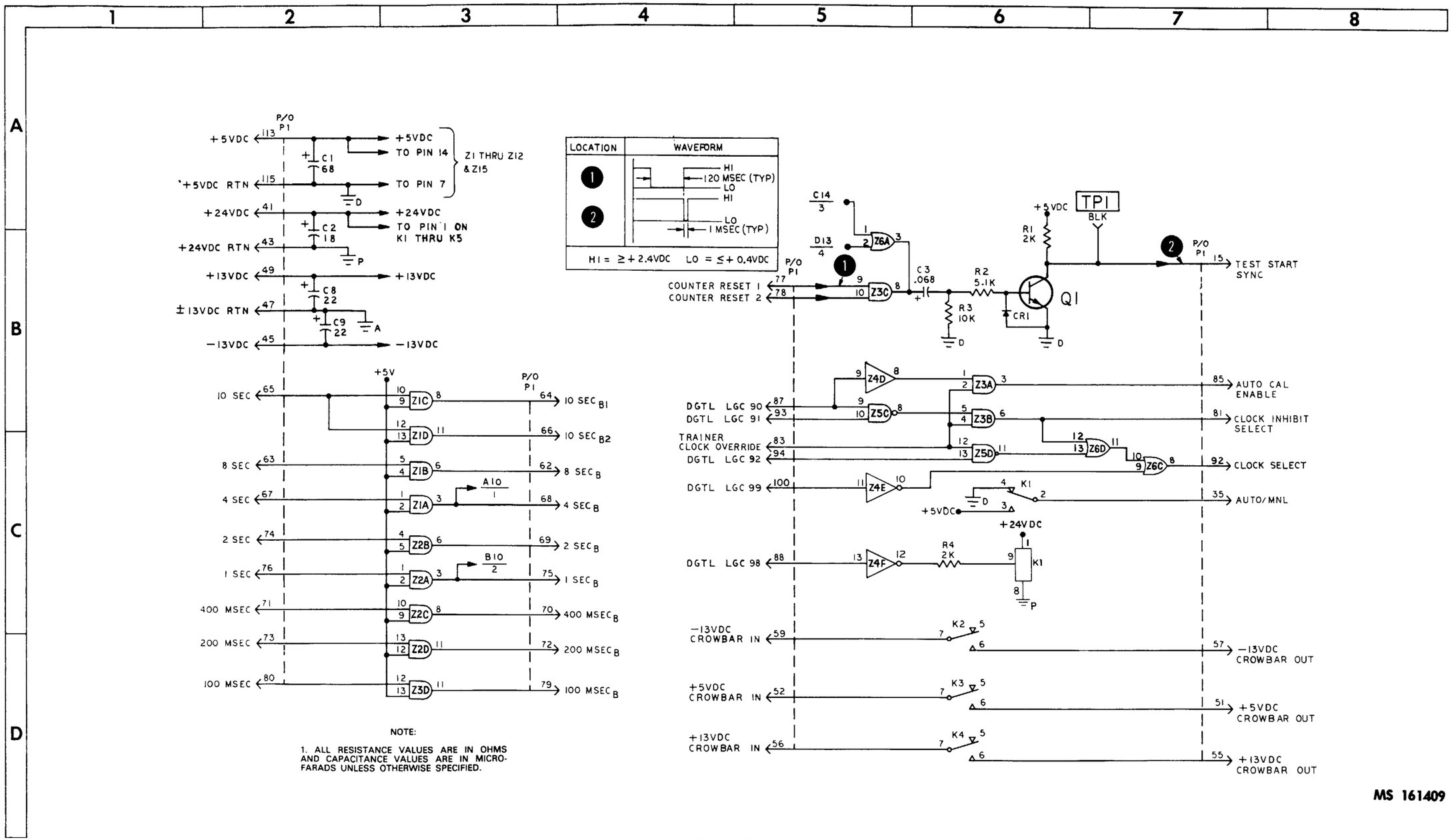


Figure 4-24. DMS-D card A23 schematic diagram (sheet 5 of 5)



NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

MS 161409

Figure 4-25. DMS-D card A24 schematic diagram (sheet 1 of 4)

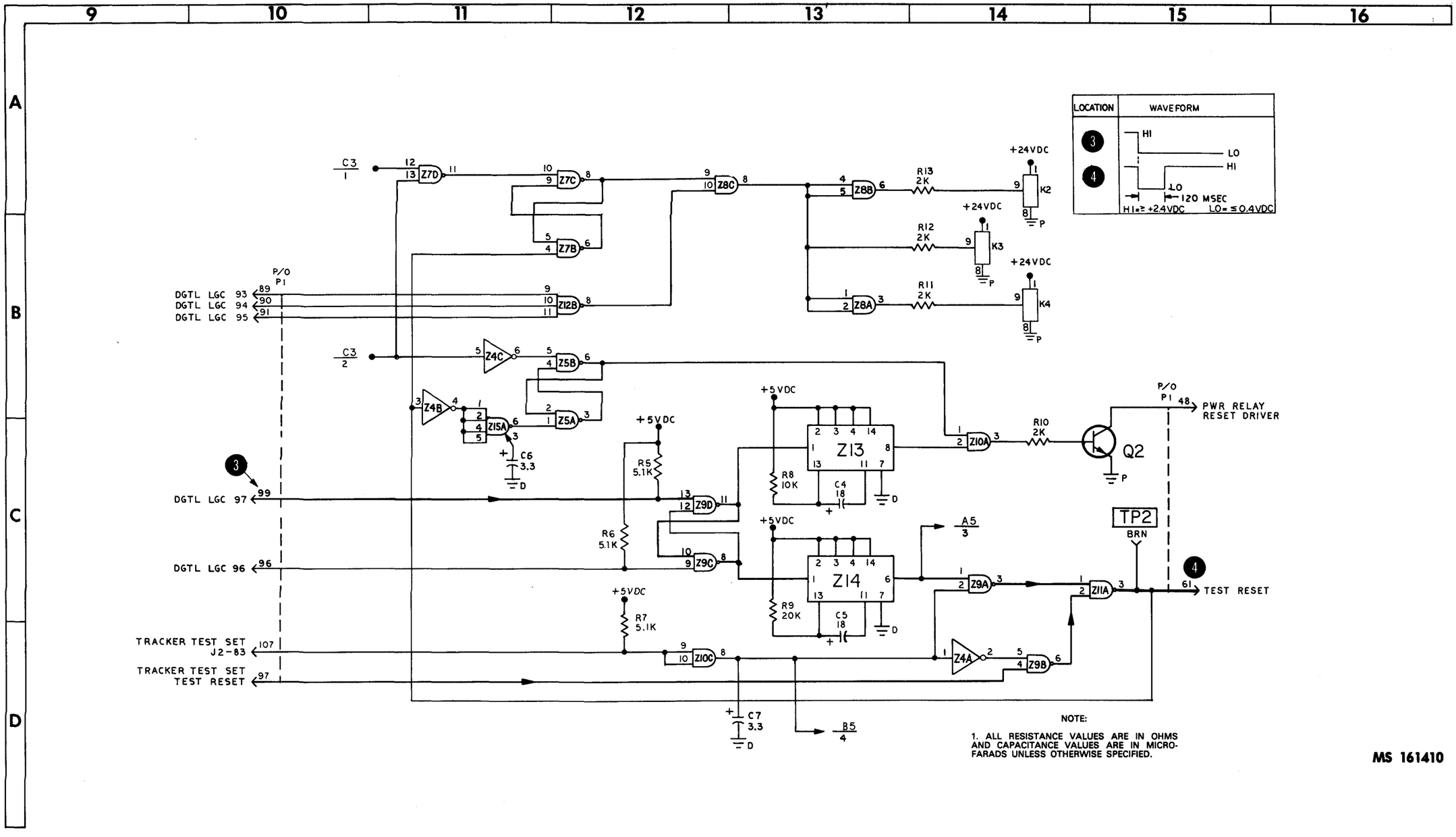
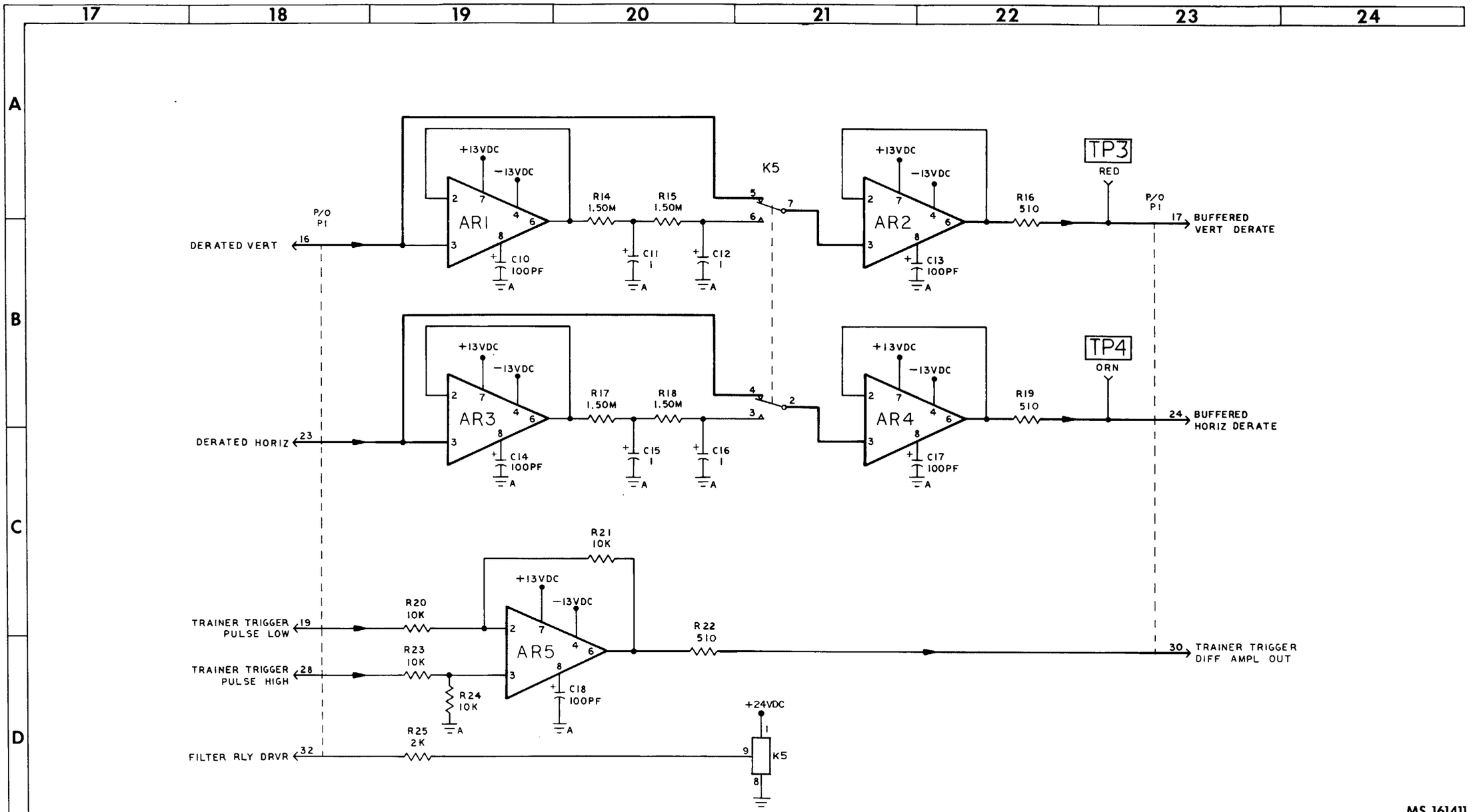


Figure 4-25. DMS-D card A24 schematic diagram (sheet 2 of 4)



MS 161411

Figure 4-25. DMS-D card A24(10275452)-schematic diagram (sheet 3 of 4)

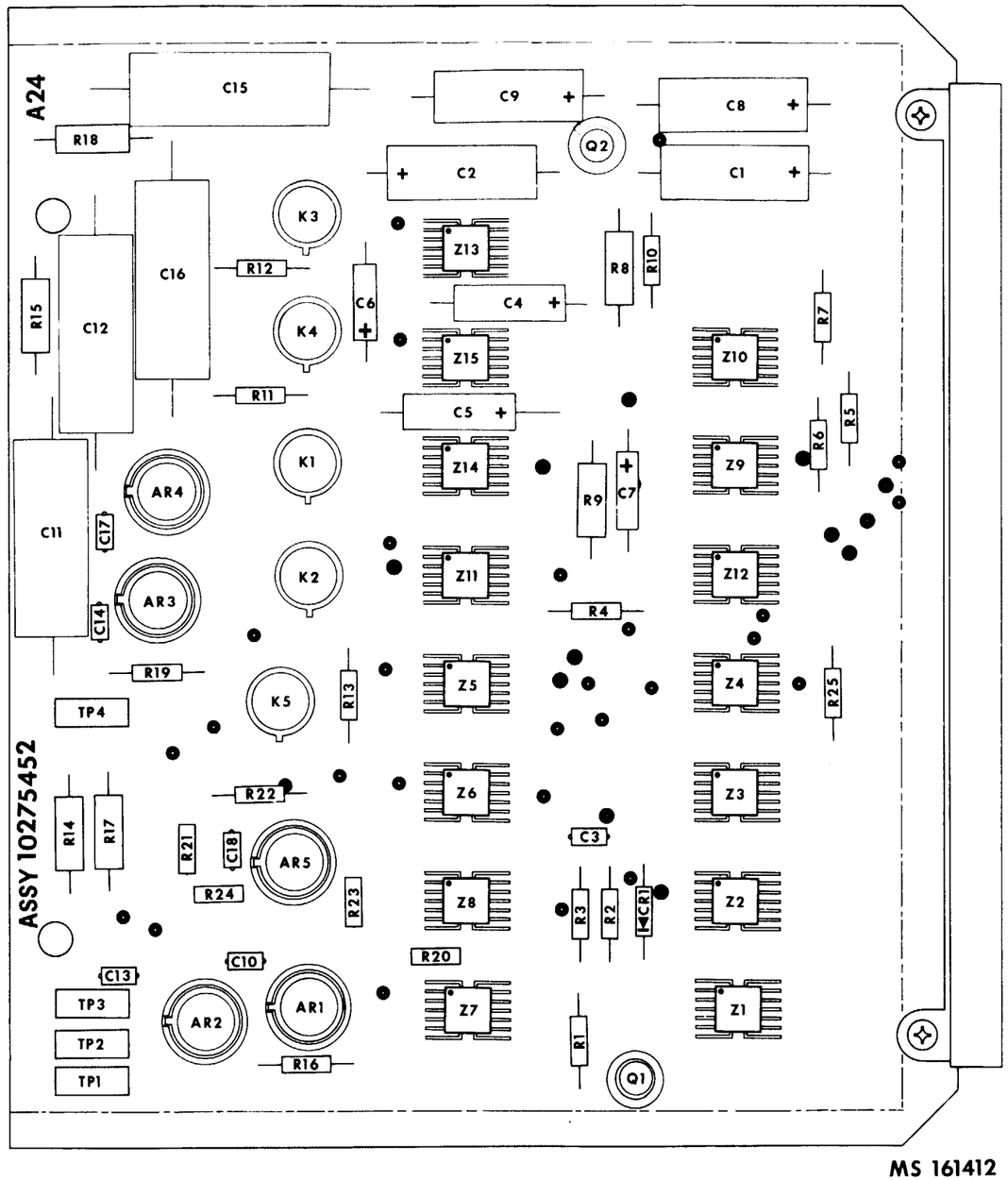
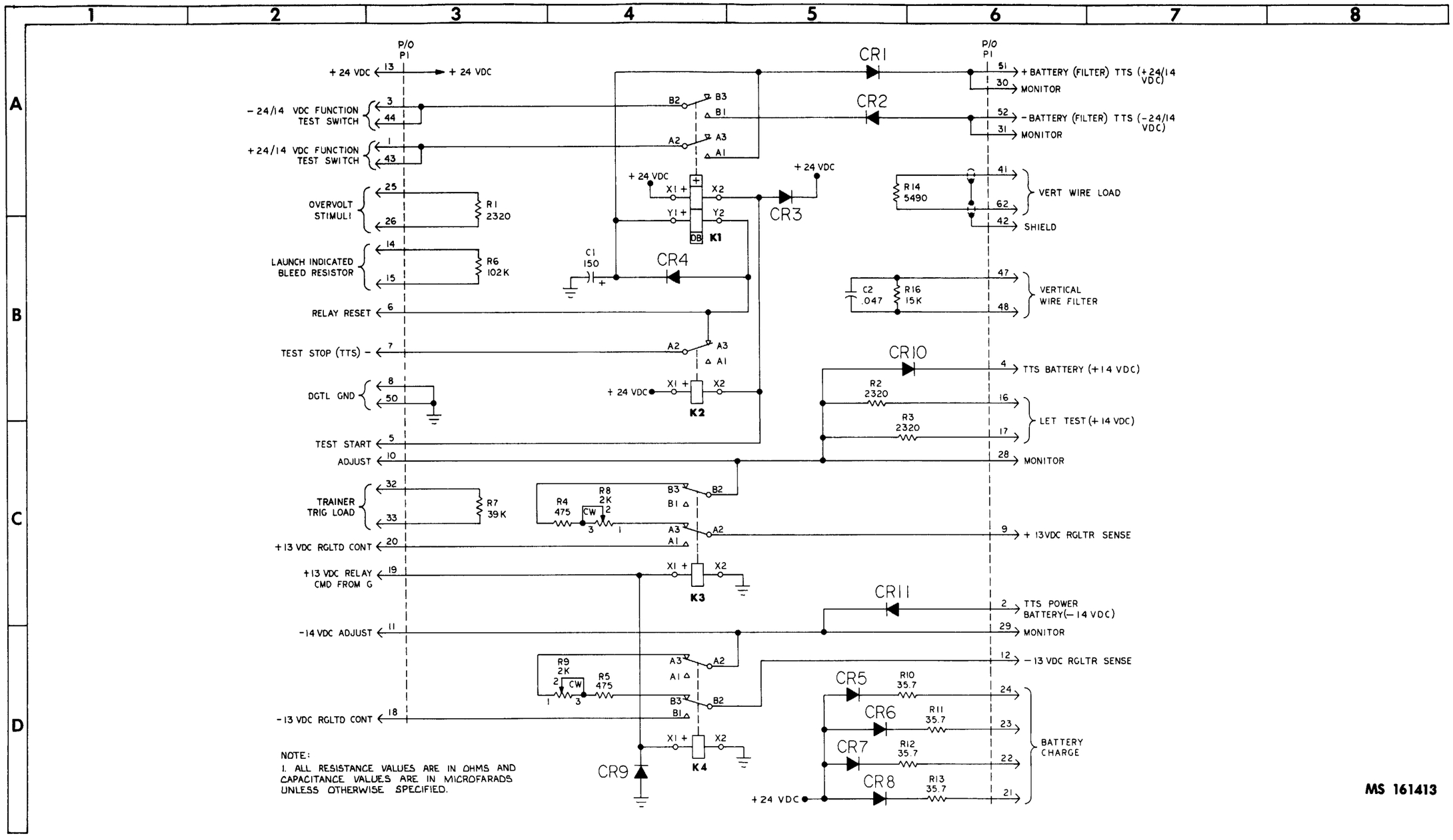


Figure 42-5. DMS-D card A24 (10275452)-schematic diagram (sheet 4 of 4)



MS 161413

Figure 4-26. DMS-D Panel Assembly A25-Schematic Diagram

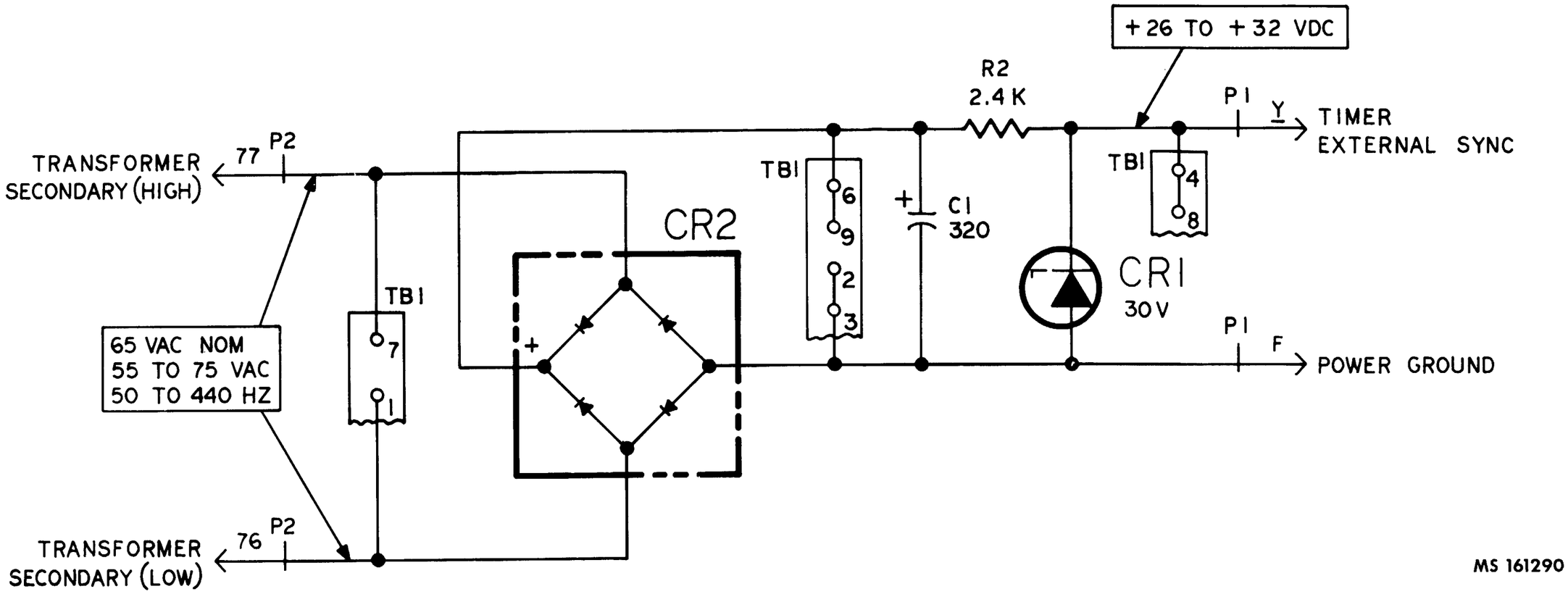


Figure 427. 'E' Cell sync adapter (10275038)-schematic diagram

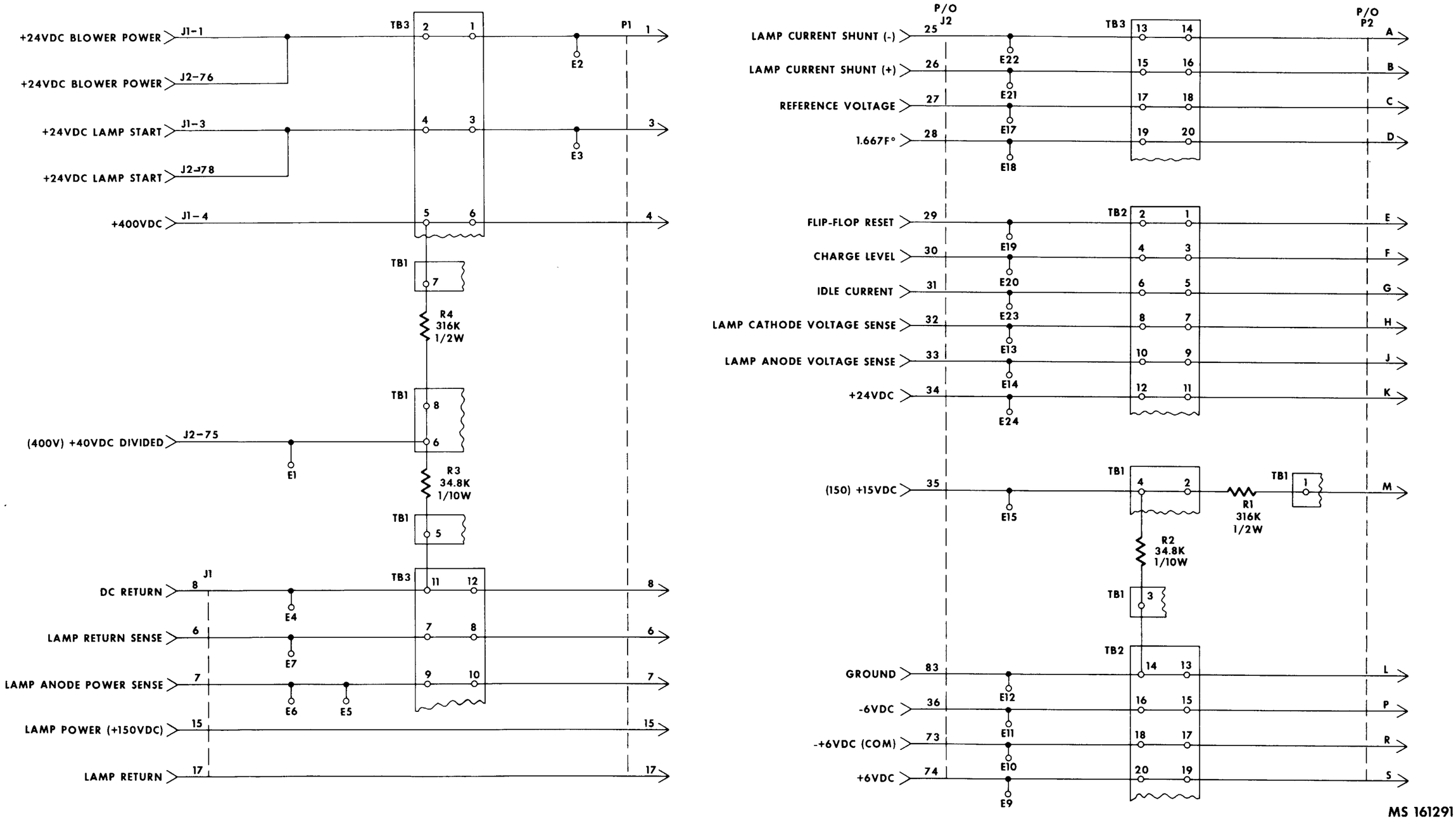


Figure 4-28. Beacon test adapter (10275448) - schematic diagram

CHAPTER 5

MK-1633 SCHEMATIC DIAGRAMS

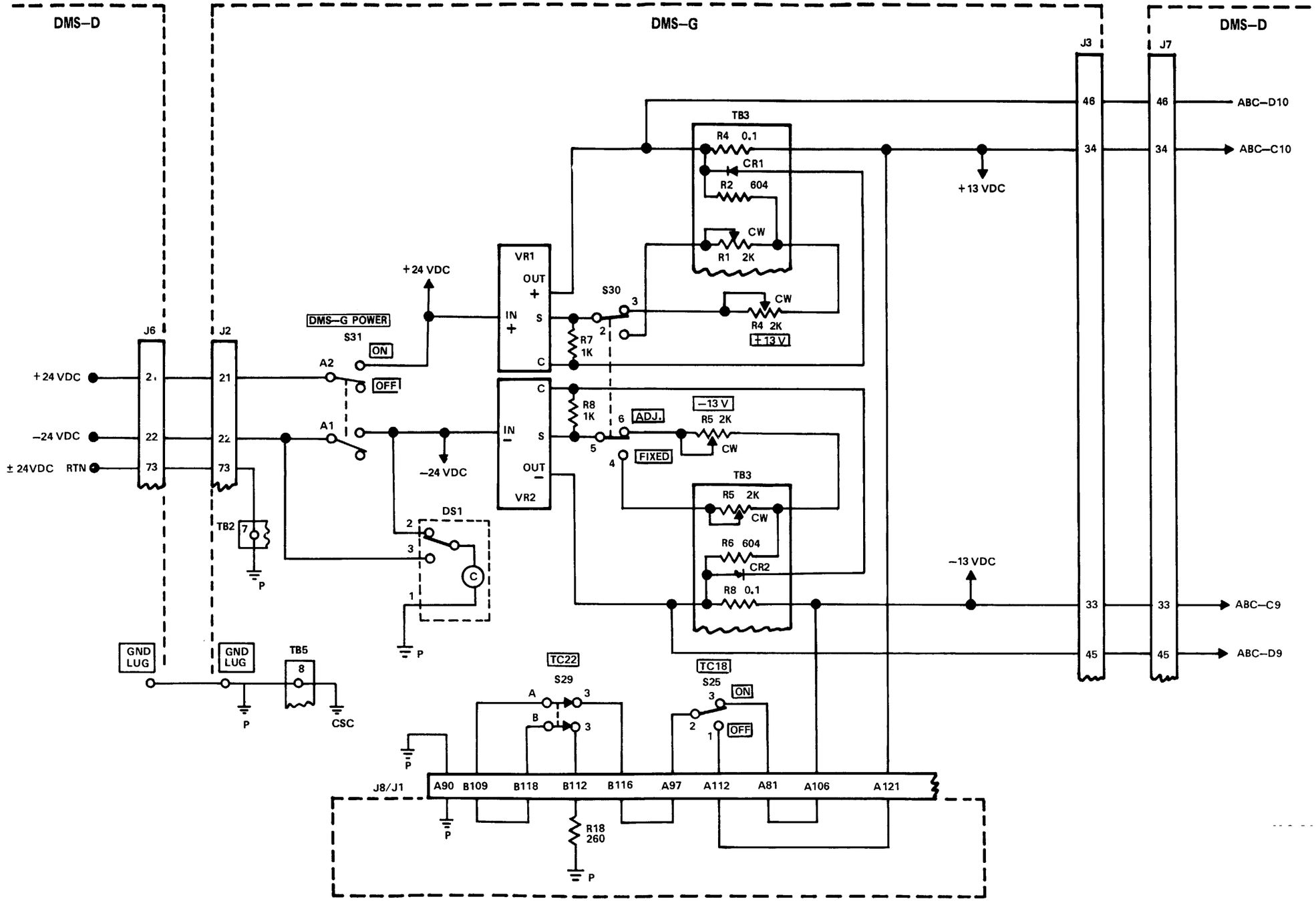


Figure 5-1. DMS-G Interface diagram (sheet 1 of 10)

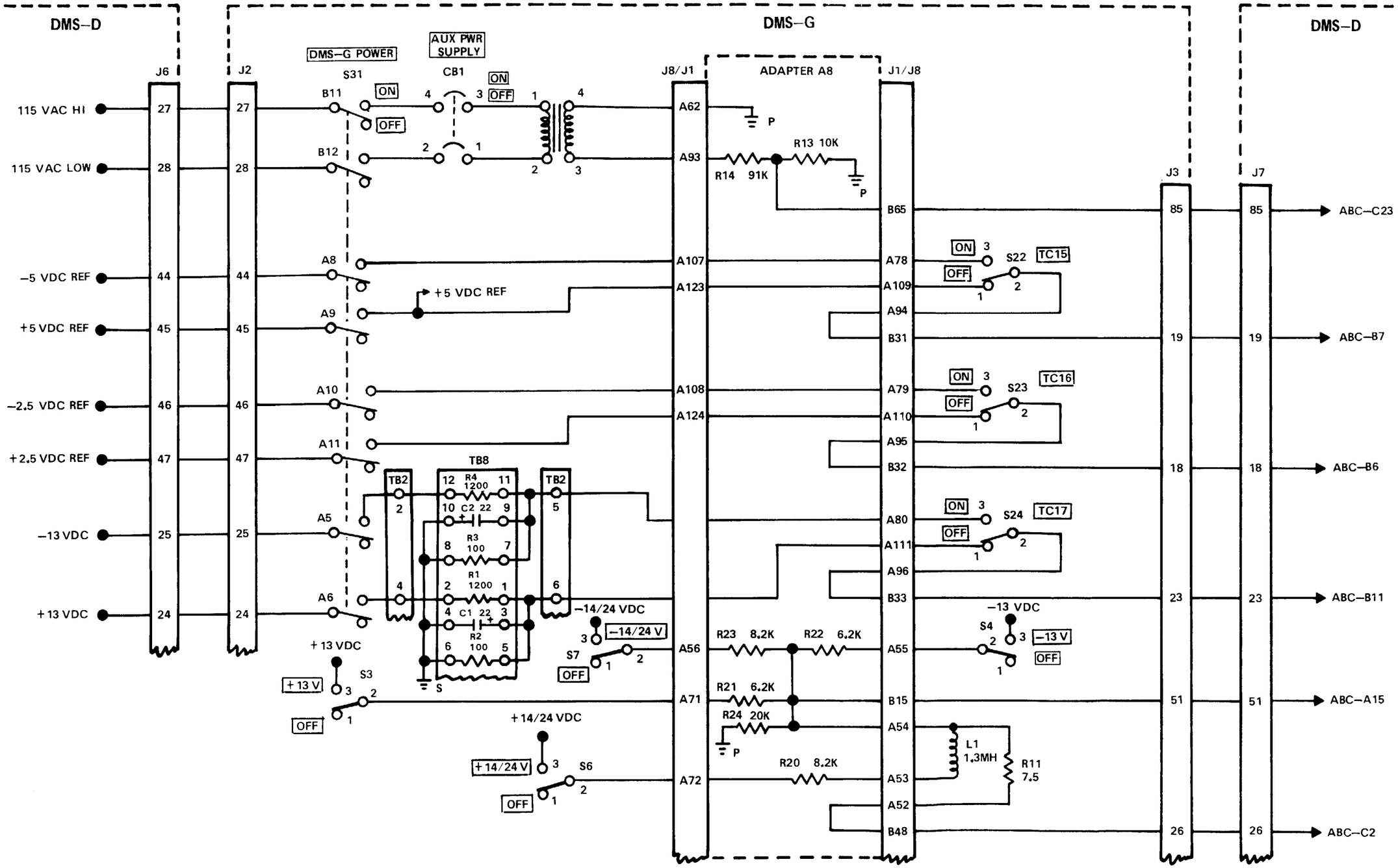


Figure 5-1. DMS-G interface diagram (sheet 2 of 10)

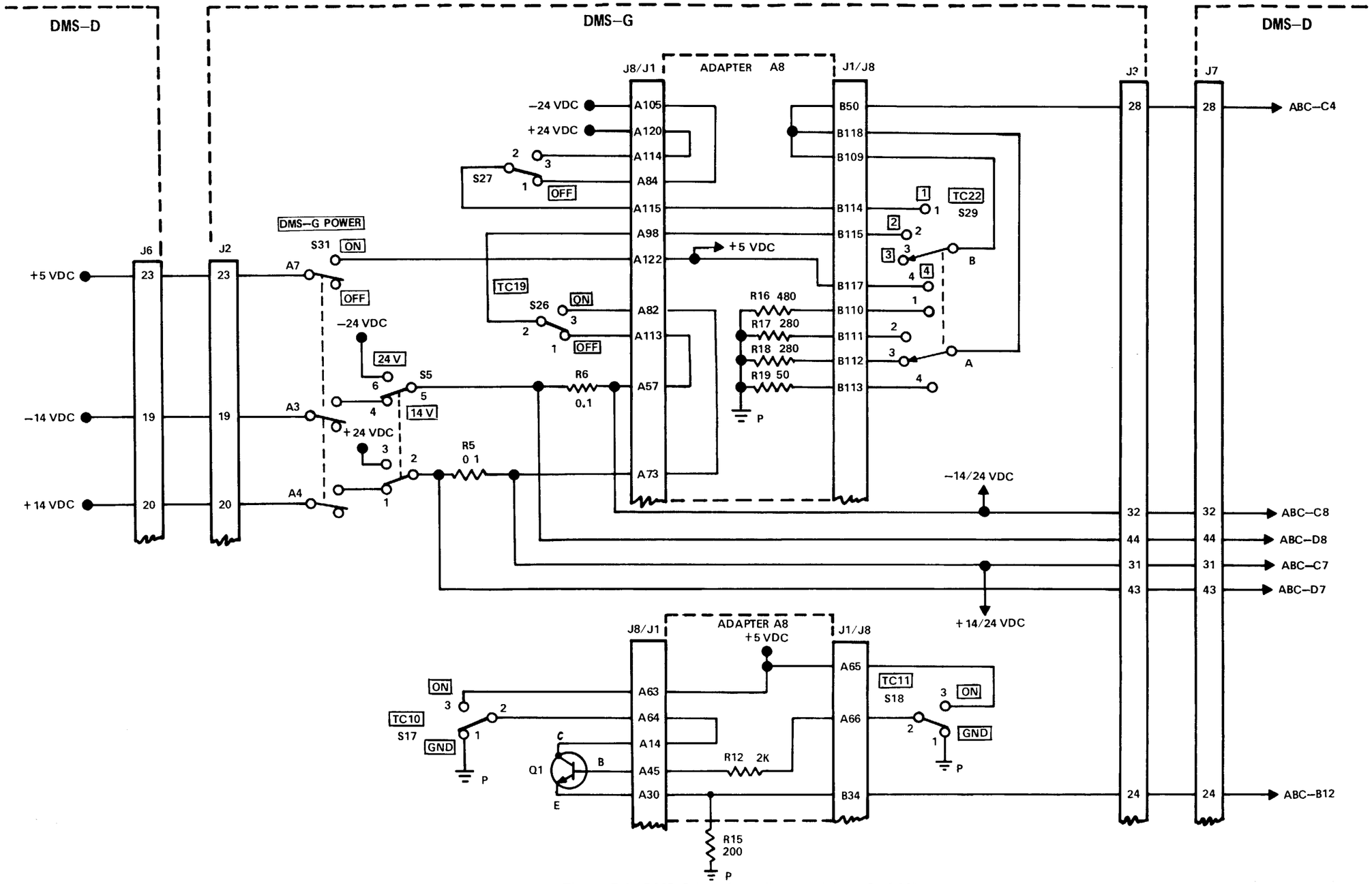


Figure 5-1. DMS-G interface diagram (sheet 3 of 10)

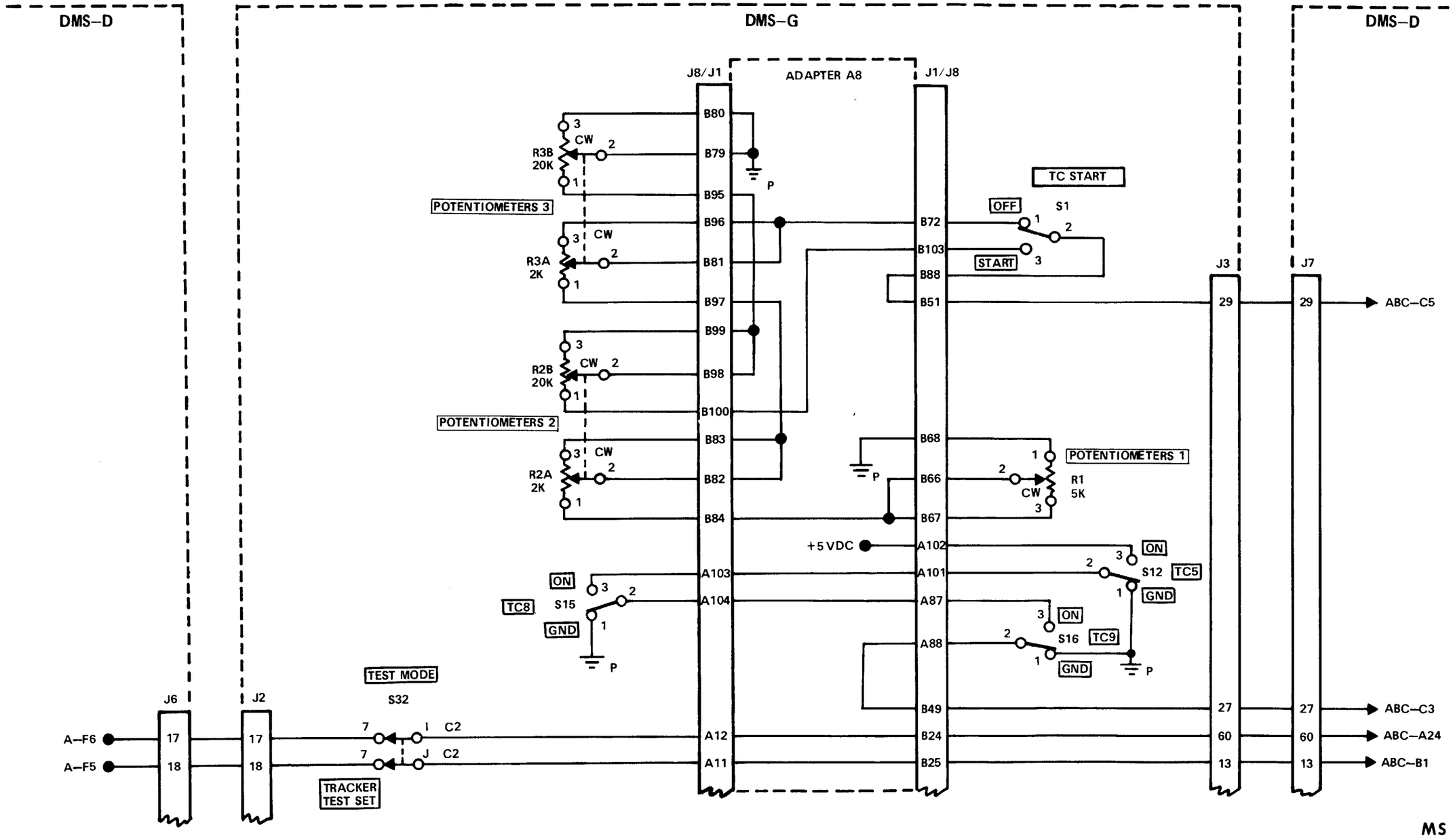


Figure 5-1. DMS-G interface diagram (sheet 4 of 10)

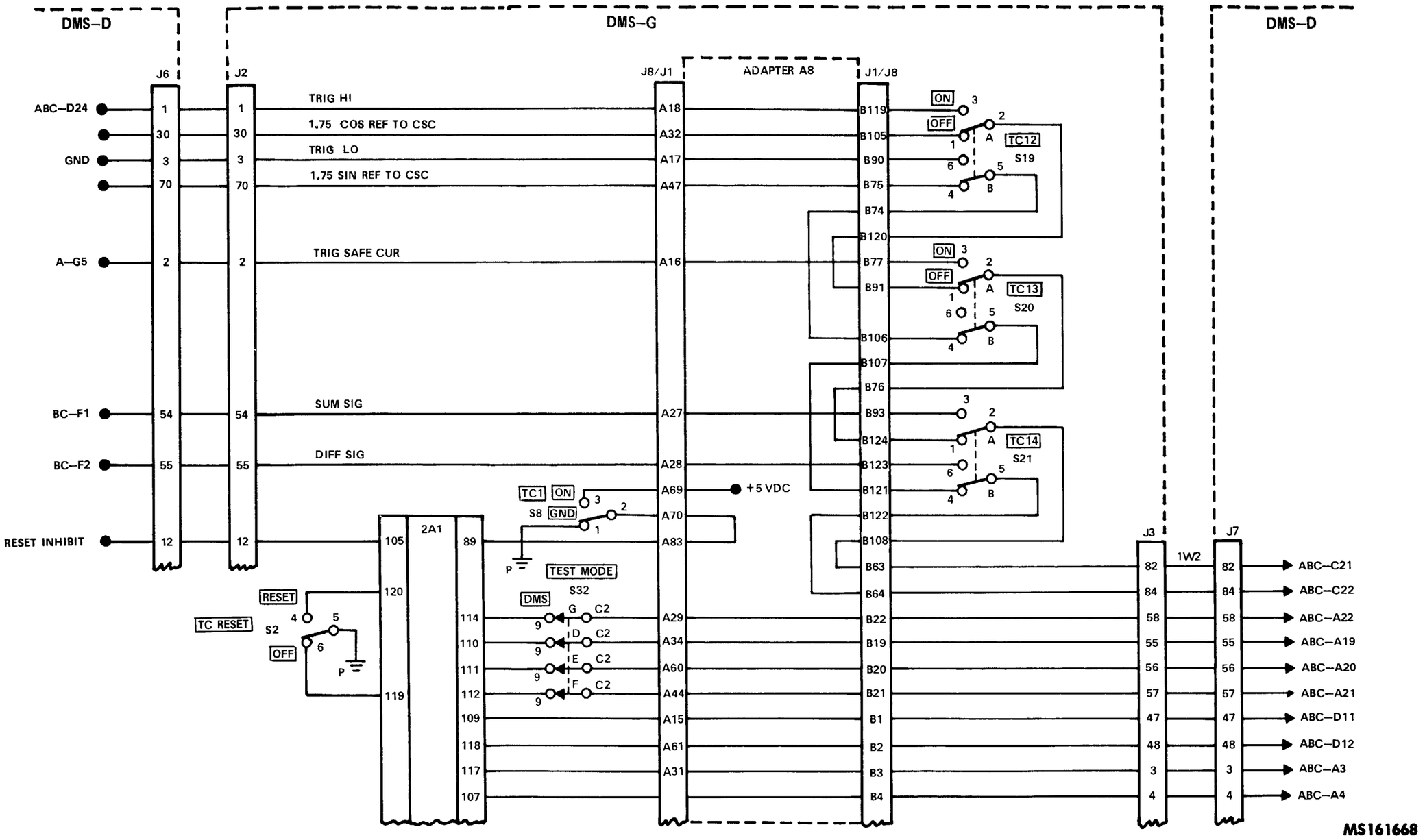


Figure 5-1. DMS-G interface diagram (sheet 5 of 10)

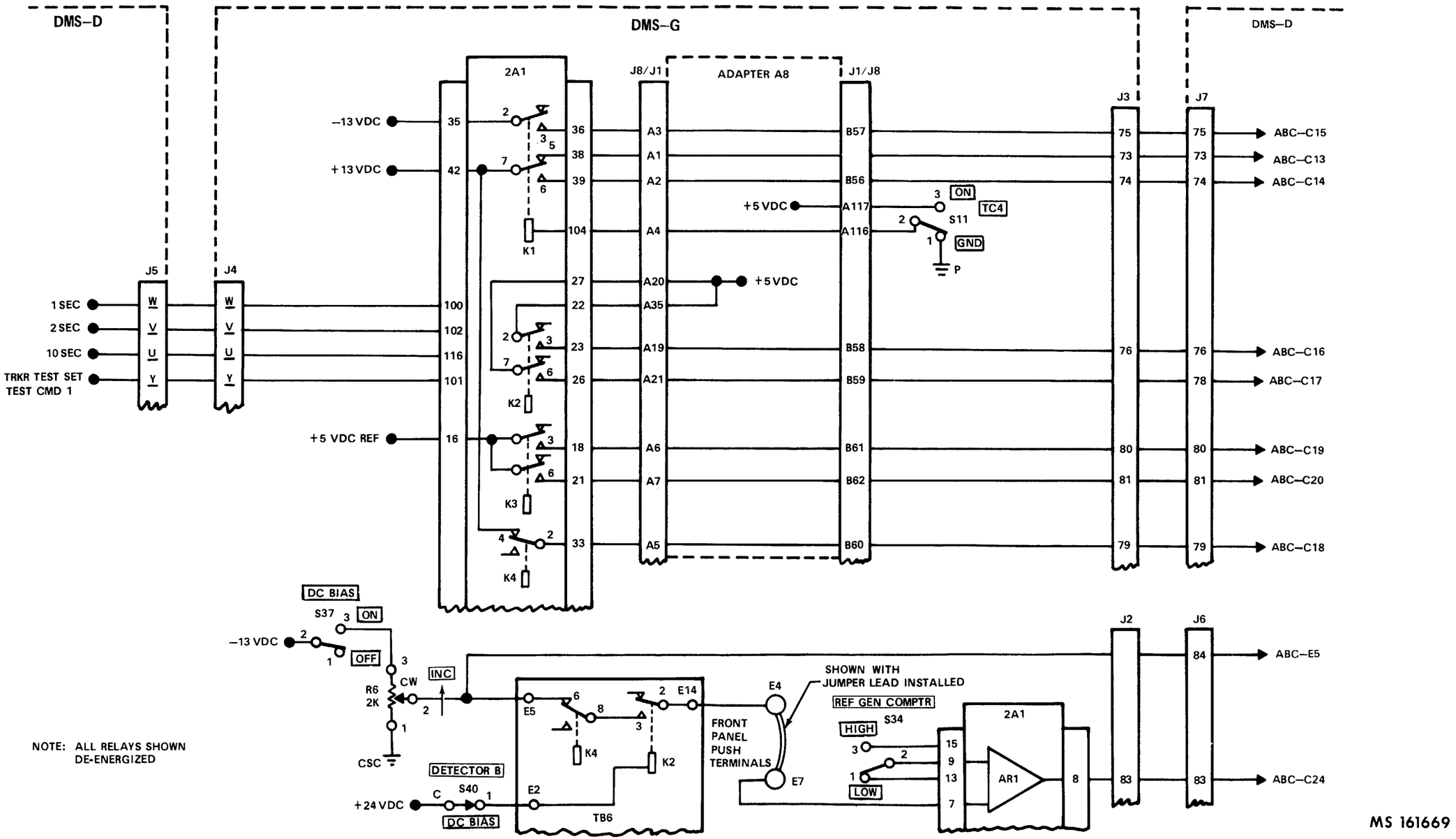


Figure 5-1. DMS-G interface diagram (sheet 6 of 10)

Figure 5-1. DMS-G interface diagram (sheet 6 of 10)

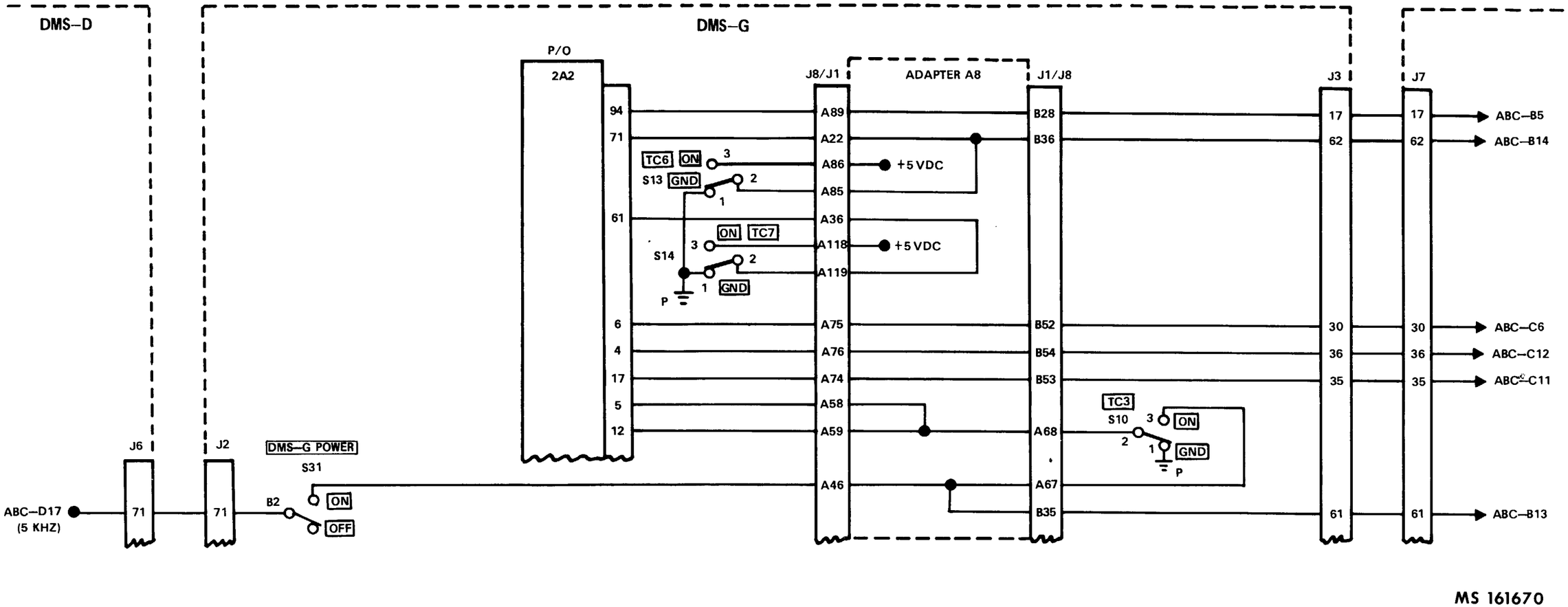
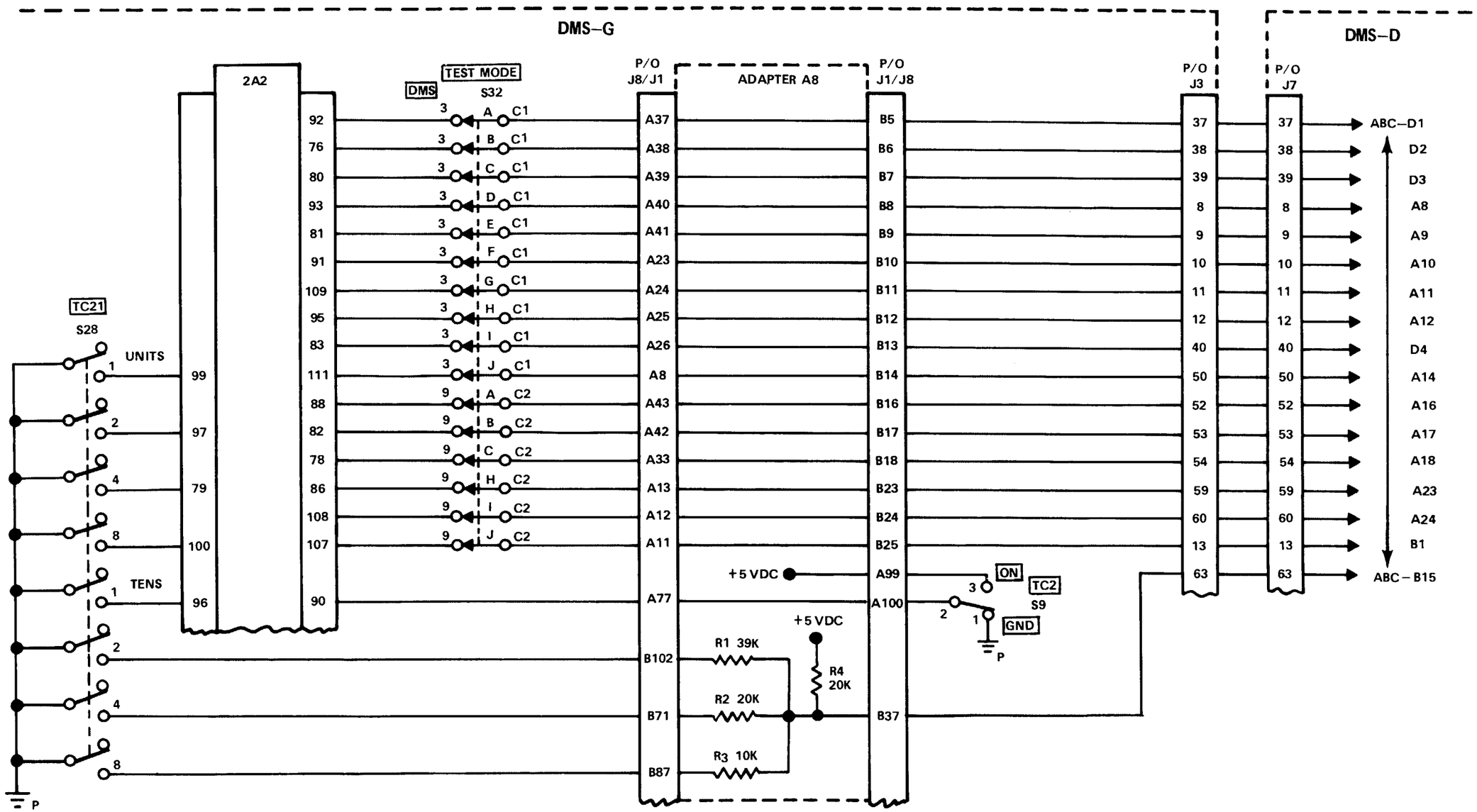


Figure 5-1. DMS-G interface diagram (sheet 7 of 10)



MS 161671

Figure 5-1. DMS-G Interface diagram (sheet 8 of 10)

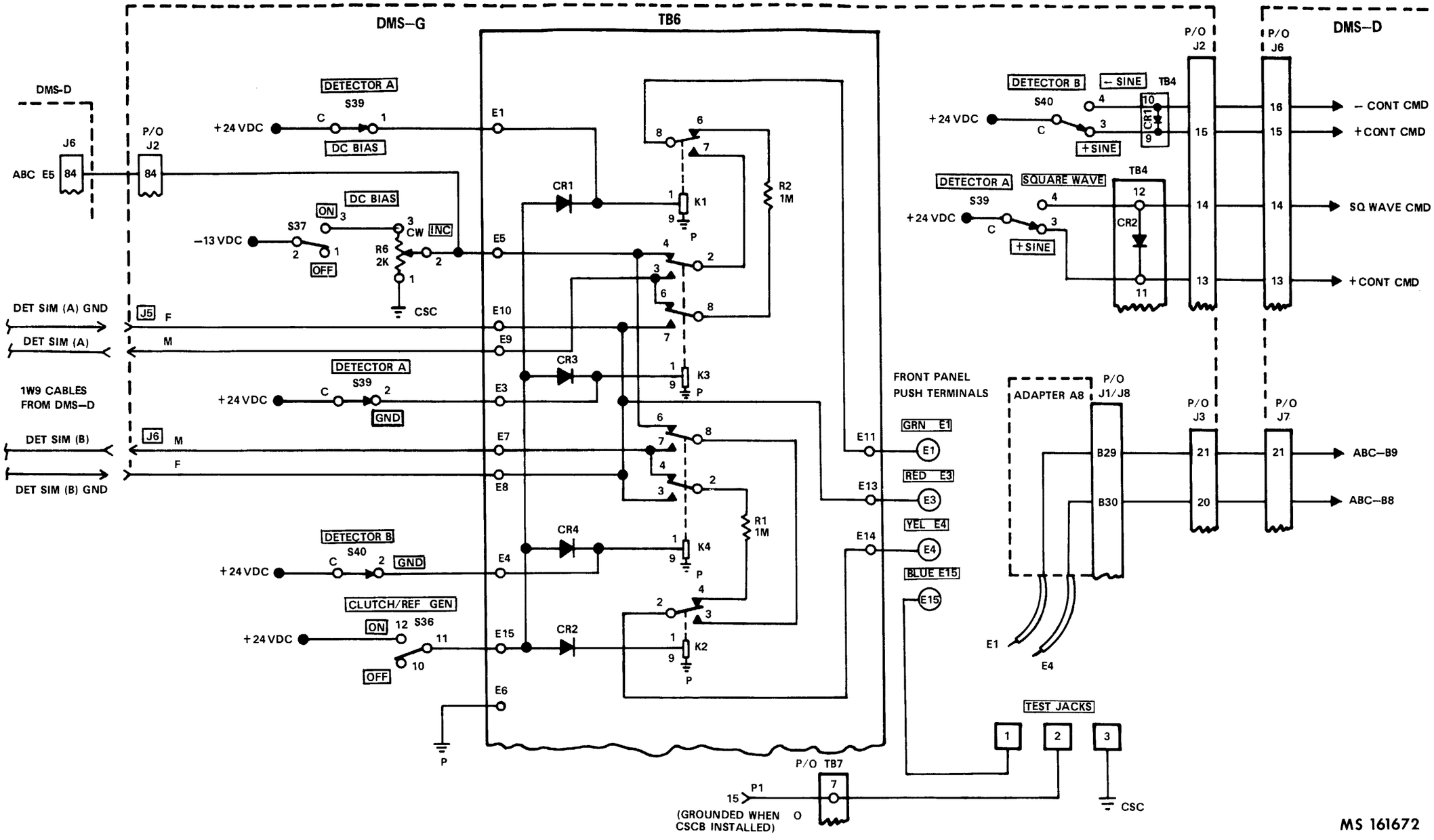


Figure 5-1. DMS-G Interface diagram (sheet 9 of 10)

TM9-4935-677-34-2

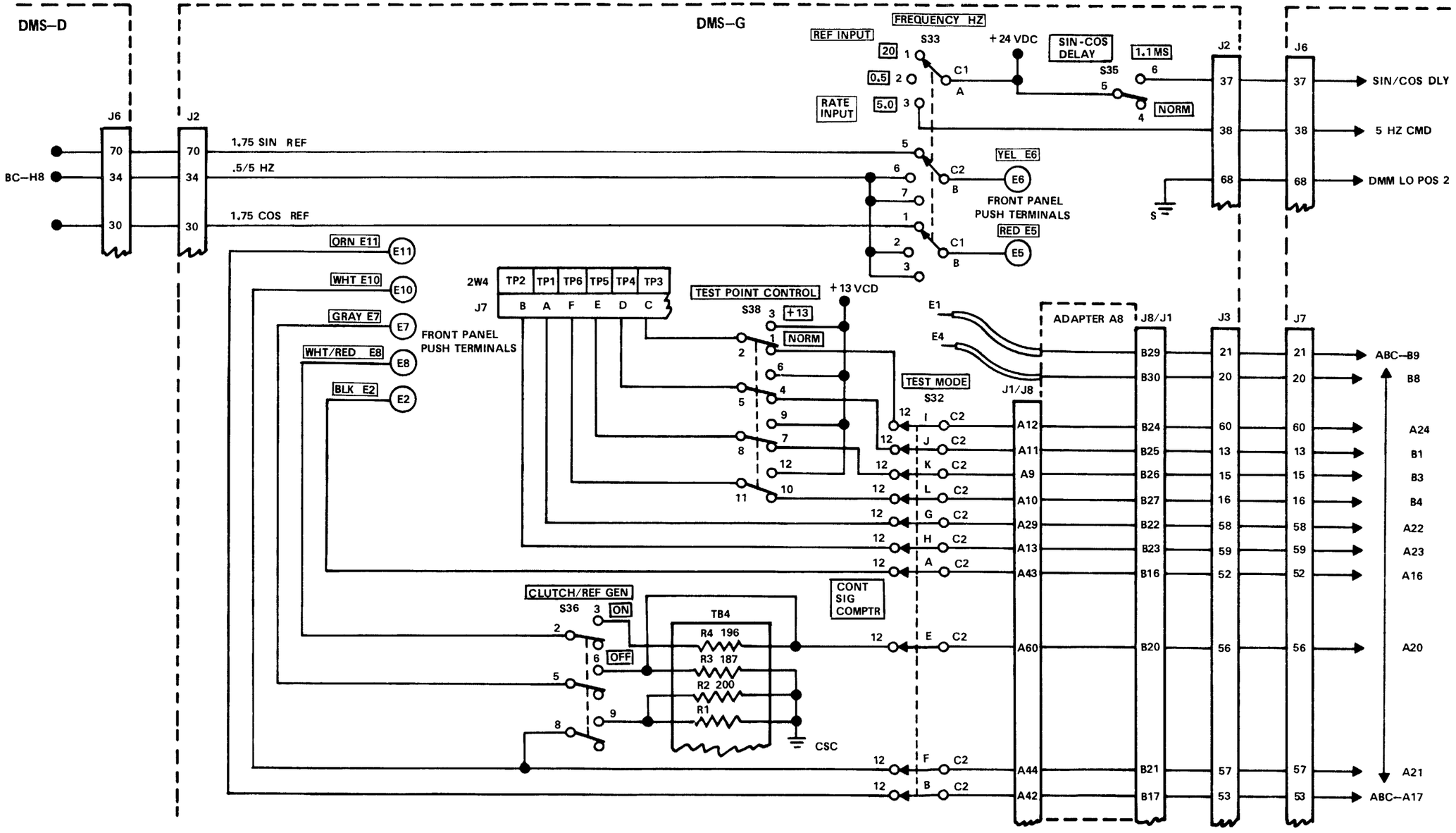


Figure 5-1. DMS-G Interface diagram (sheet 10 of 10)

INDEX	
REFERENCE DESIGNATION	SHEET NUMBER
A1	10
A2	10
CB1	2
DS1	2
E1	9
E2	9
E3	9
E4	9
E5	8
E6	8
E7	9
E8	↓
E9	
E10	
E11	
E12	
E13	
E14	9
E15	8
E16	8
E17	8
E18	8
E19	9
E20	9
E21	9
E22	9
E30	3
E31 – E37	7
E39 – E46	7
E47	3
E48,E49	7
E50	3
E51	8
E52	2
E53,E54,E55	3
J2	2,3,6,7,8,9,10
J3	2,4,7
J4	6,7,10
J5	9
J6	9
J7	6,9
J8	2,3,4,5,6,7,8,10
L1	5
P1	8
Q1	5
R1	5
R2	5
R3	5
R4	2
R5	2
R6	9
R7	2

INDEX	
REFERENCE DESIGNATION	SHEET NUMBER
R8	2
R9	8
R10	8
R11	5
S1	4
S2	4
S3	2
S4	2
S5	2
S6	2
S7	2
S8	4
S9	↓
S10	
S11	
S12	
S13	
S14	
S15	
S16	
S17	
S18	
S19	
S20	
S21	
S22	
S23	
S24	
S25	
S26	
S27	4
S28	5
S29	5
S30	2
S31	2,3
S32	6,7
S33	8
S34	10
S35	9
S36	9
S37	9
S38	9
S39	9
S40	9
T1	2
TB1	2,3
TB2	2,3
TB3	2
TB4	2,9
TB5	2,8
TB6	9
TB7	8
TB8	3
VR1	2
VR2	2
W5	2,3,4,5,6,7,8,10
W5J1	2,3,4,5,6,7,8,10
W5P1	2,3,4,5,6,7,8,10
XA1	10
XA2	10
XA3	10

NOTES:
1. ALL VALUES IN OHMS UNLESS OTHERWISE SPECIFIED.
2. LOWER CASE LETTERS ARE SHOWN AS UNDERLINED UPPER CASE LETTERS.
3. NON-STANDARD ABBREVIATIONS:
   - 3.1 FR G MEANS FROM DMS-G.
   - 3.2 FR D MEANS FROM DMS-D
   - 3.3 TO D MEANS TO DMS-D
   - 3.4 ABC- MEANS DMS-D SELECTORS A. B & C- POSITION XXX.
   - 3.5 CSC MEANS CONTROL. SIGNAL COMPARATOR.
   - 3.6 TC MEANS TEST CONTROL
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION. PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATION(S).
5. ALL WAFER SWITCH PIN NUMBERS ARE MARKED ON THE DECKS. DECK NUMBERS ARE IDENTIFIED BY BEGINNING WITH THE FIRST ALPHA OR NUMERIC DIGIT AT THE KNOB END.

TC-21 SWITCH PIN NUMBERS ARE IDENTIFIED AS SHOWN BELOW:

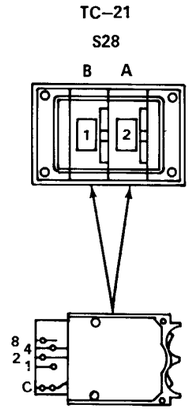
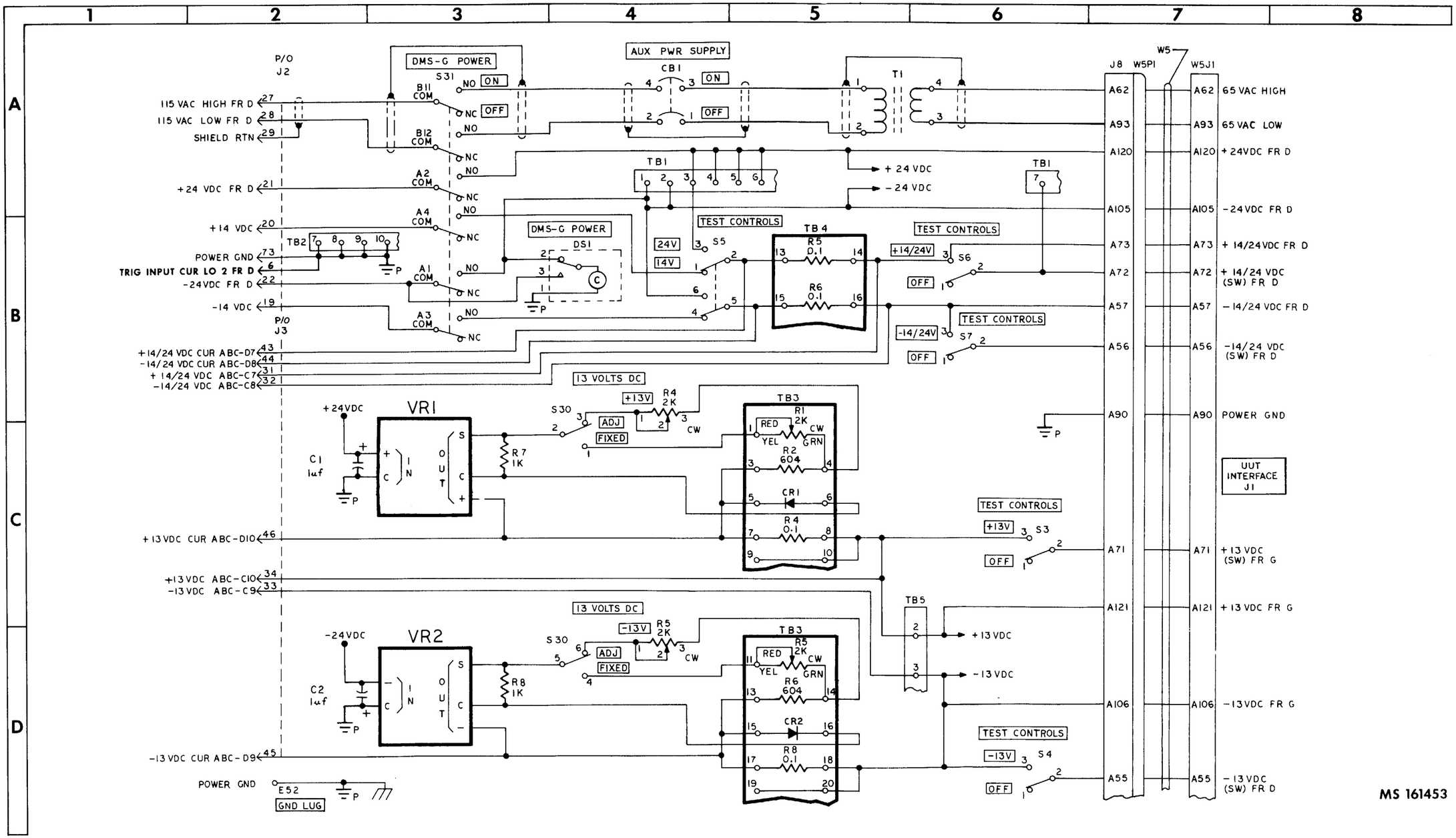


Figure 5-2. DMS-G - schematic diagram (sheet 1 of 10)



MS 161453

Figure 5-2. DMS-G - schematic diagram (sheet 2 of 10)

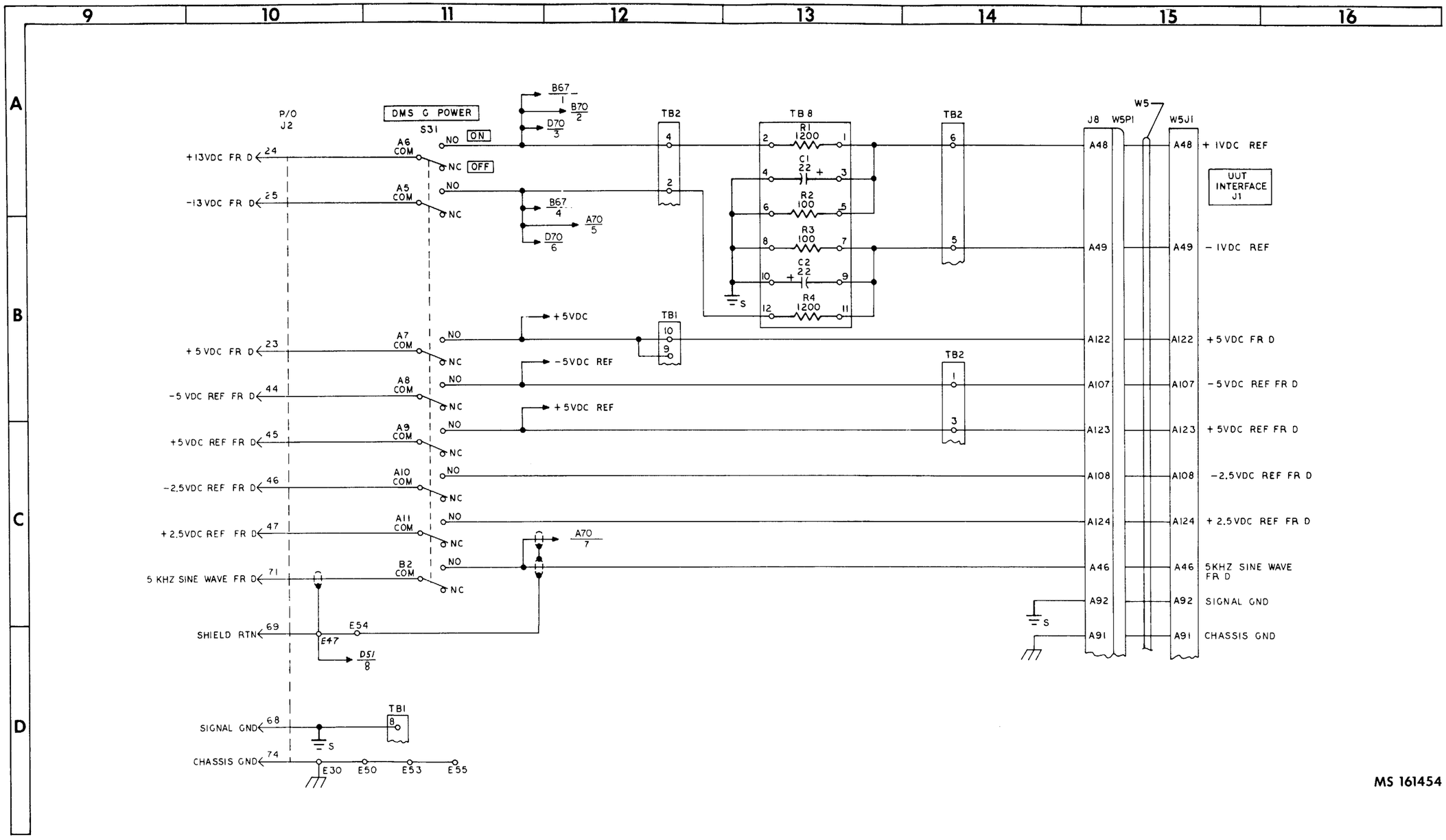


Figure 5-2. DMS-G - schematic diagram (sheet 3 of 10)

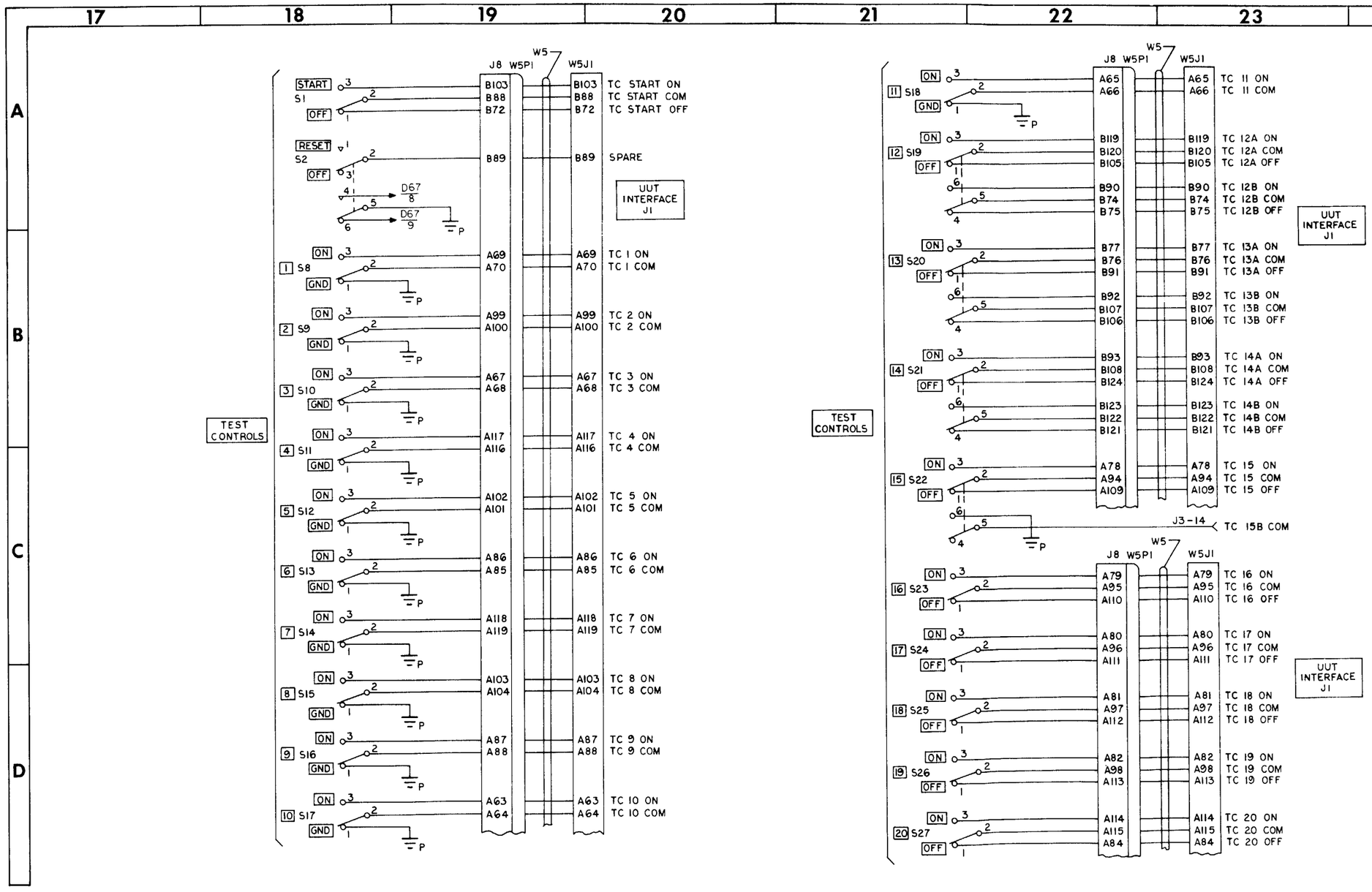


Figure 5-2. DMS-G- schematic diagram (sheet 4 of 10)

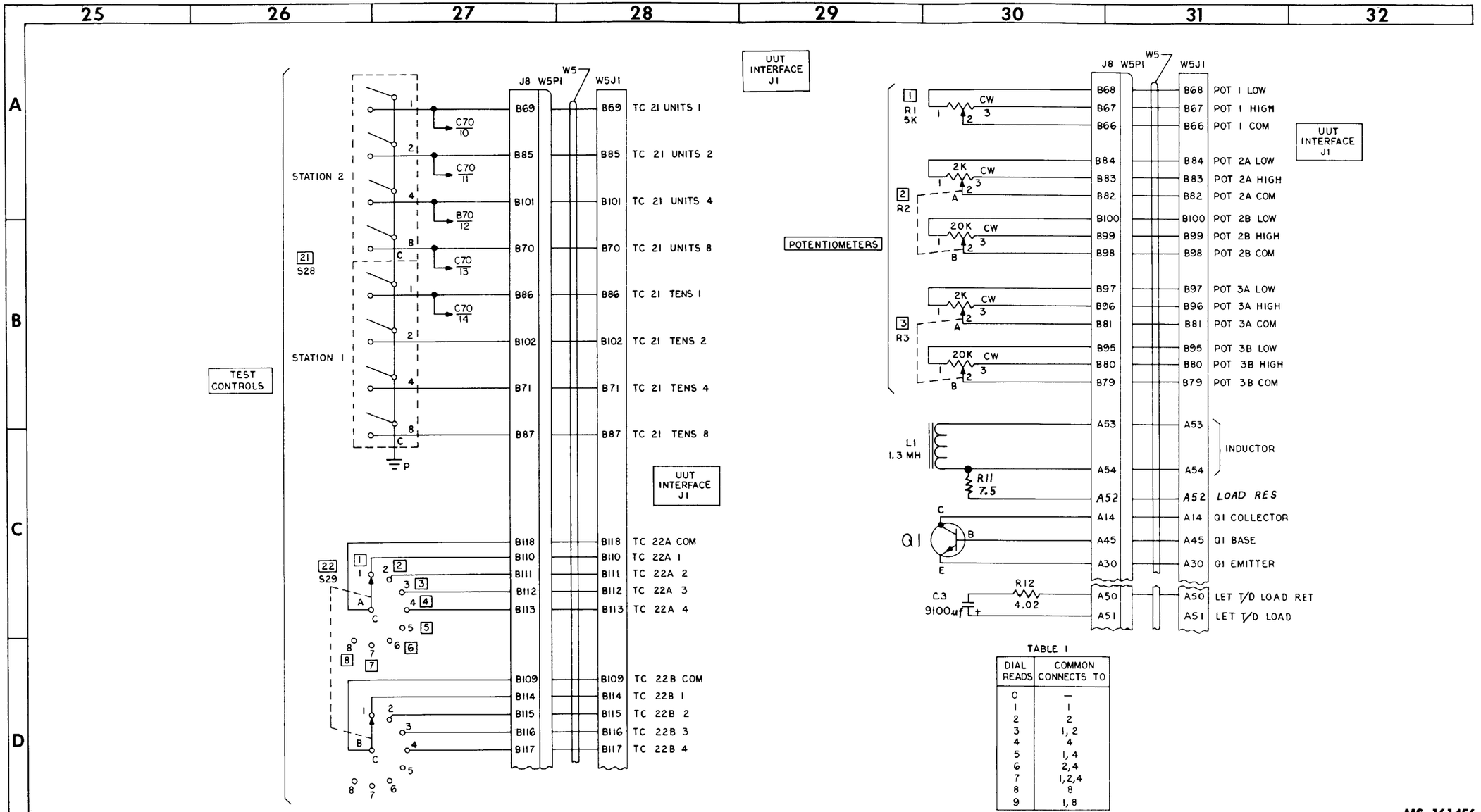


Figure 5-2. DMS-G - schematic diagram (sheet 5 of 10)

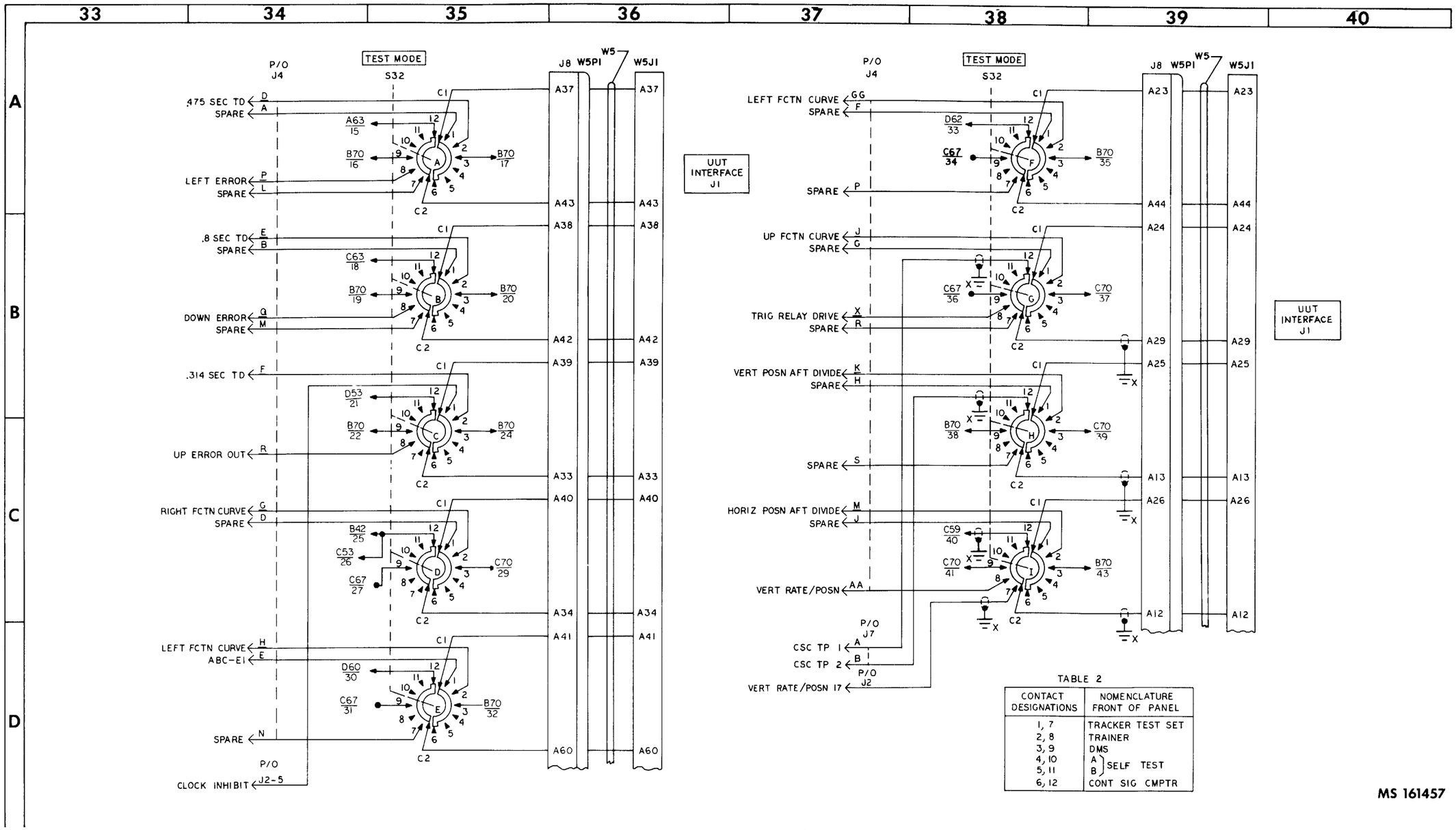


TABLE 2

CONTACT DESIGNATIONS	NOMENCLATURE FRONT OF PANEL
1, 7	TRACKER TEST SET
2, 8	TRAINER
3, 9	DMS
4, 10	A } SELF TEST
5, 11	B } SELF TEST
6, 12	CONT SIG CMPTR

MS 161457

Figure 5-2. DMS-G- schematic diagram (sheet 6 of 10)

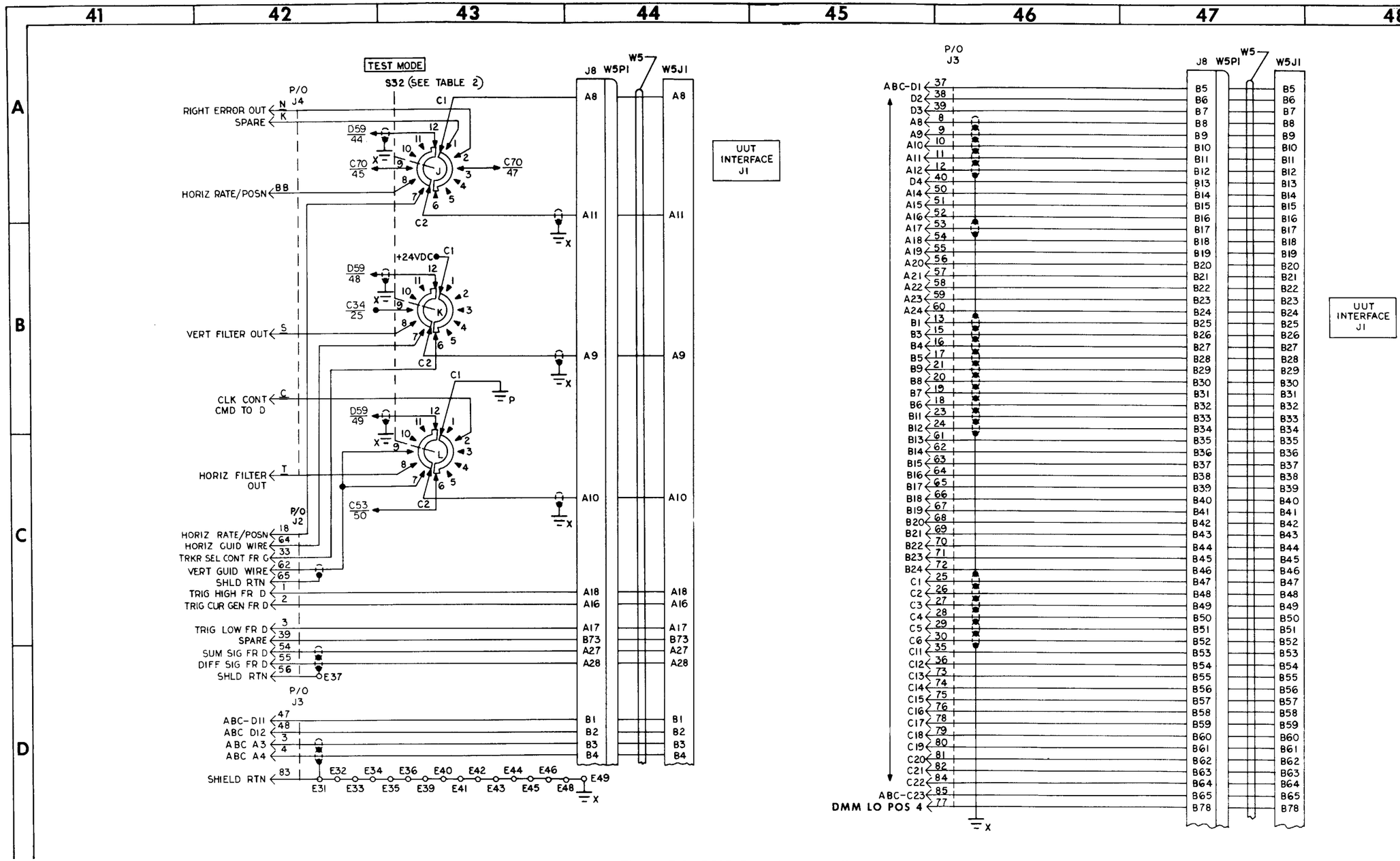


Figure 5-2. DMS-G - schematic diagram (sheet 7 of 10)

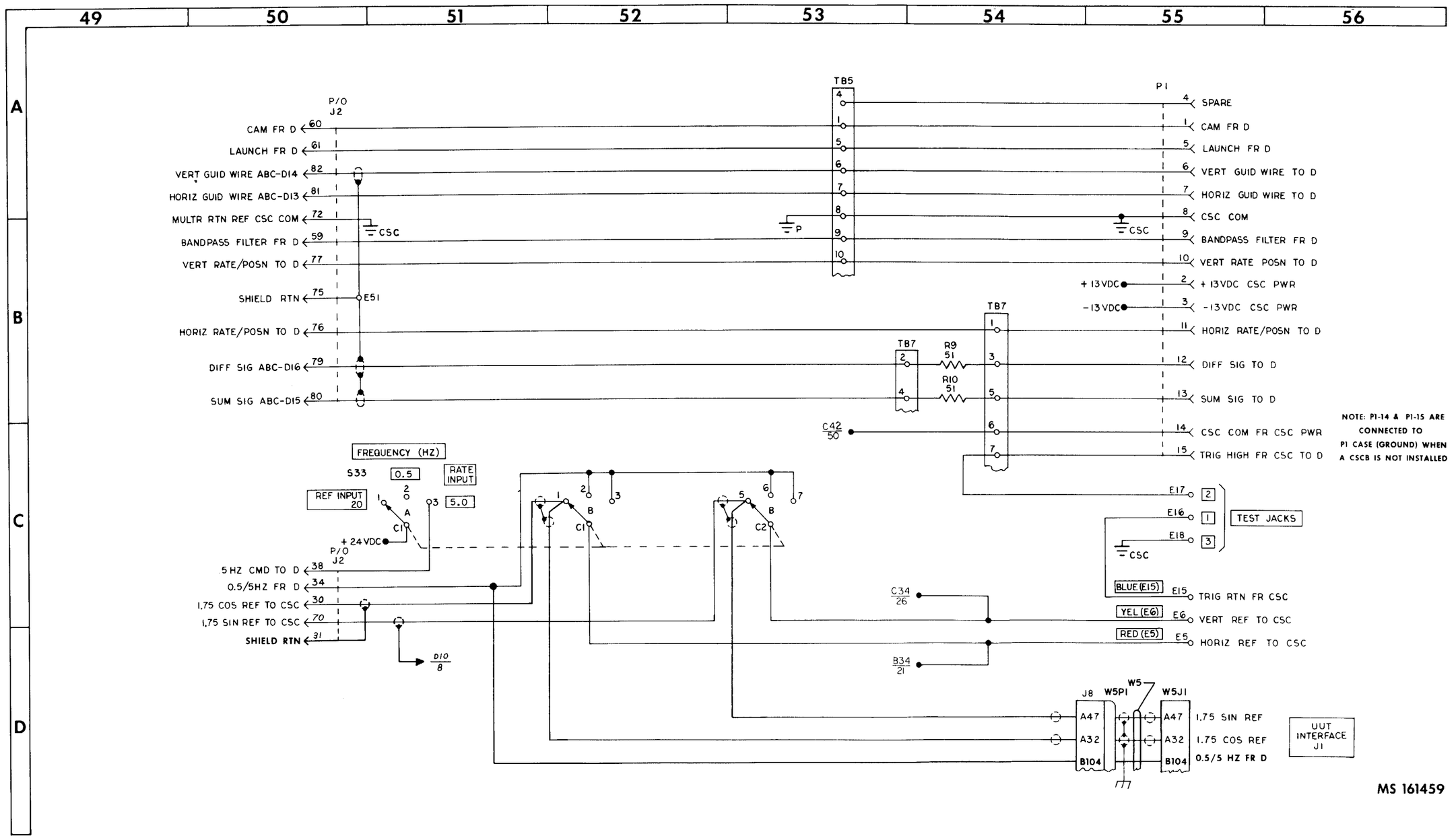


Figure 5-2. DMS-G -schematic diagram (sheet 8 of 10)

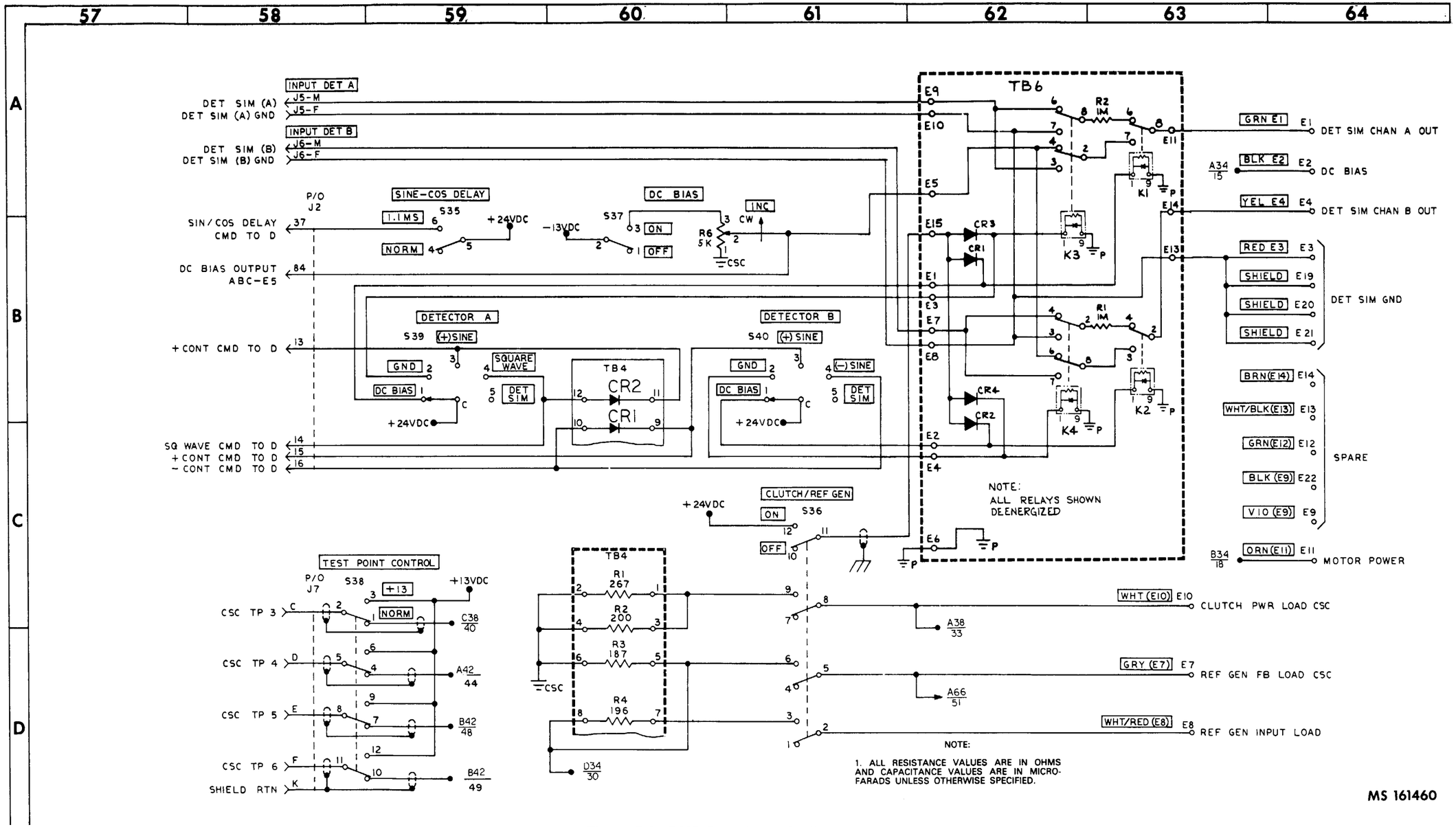
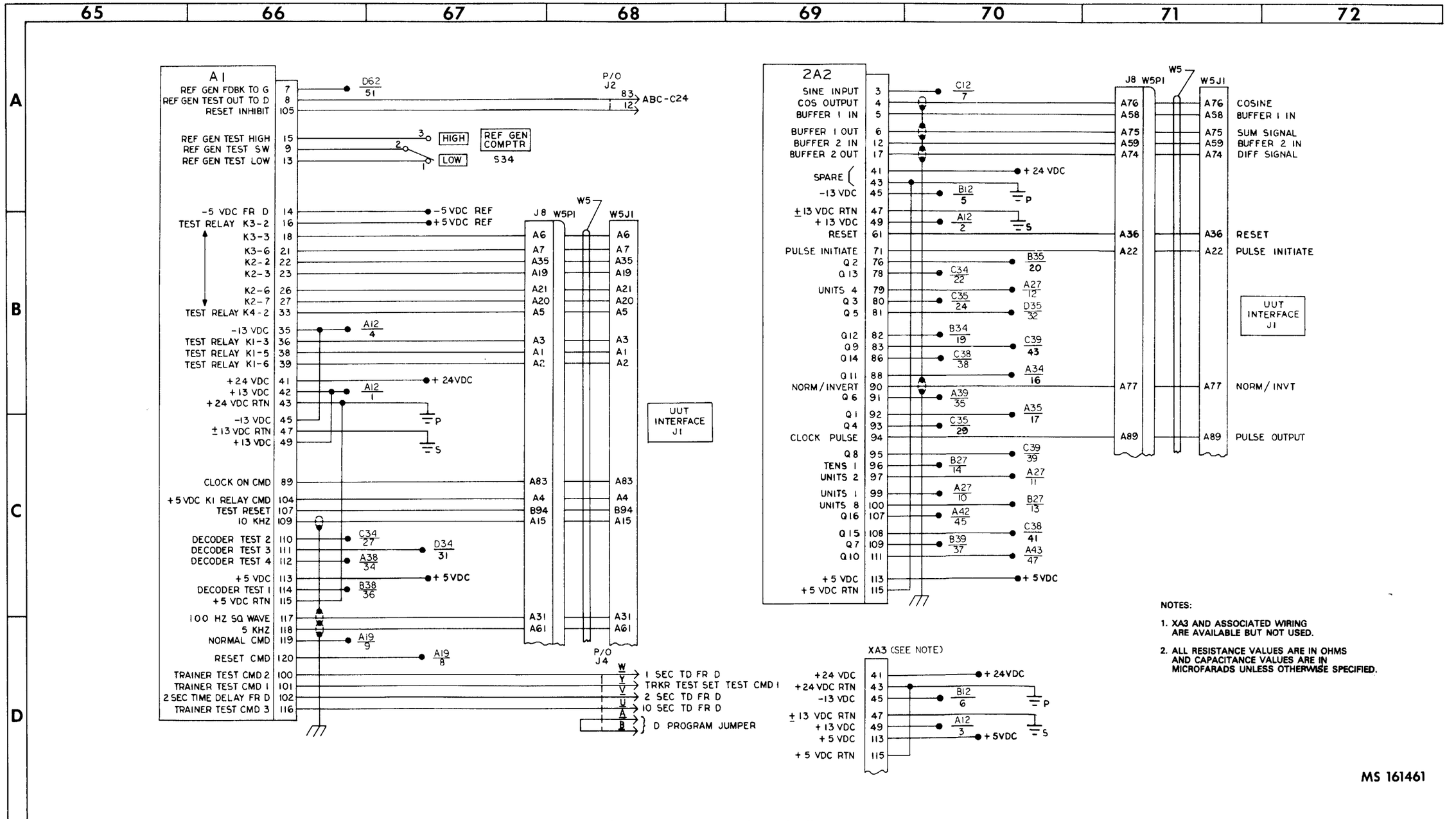


Figure 5-2. DMS-G - schematic diagram (sheet 9 of 10)



NOTES:

1. XA3 AND ASSOCIATED WIRING ARE AVAILABLE BUT NOT USED.
2. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

MS 161461

Figure 5-2 . DMS-G-schematic diagram (sheet 10 of 10)

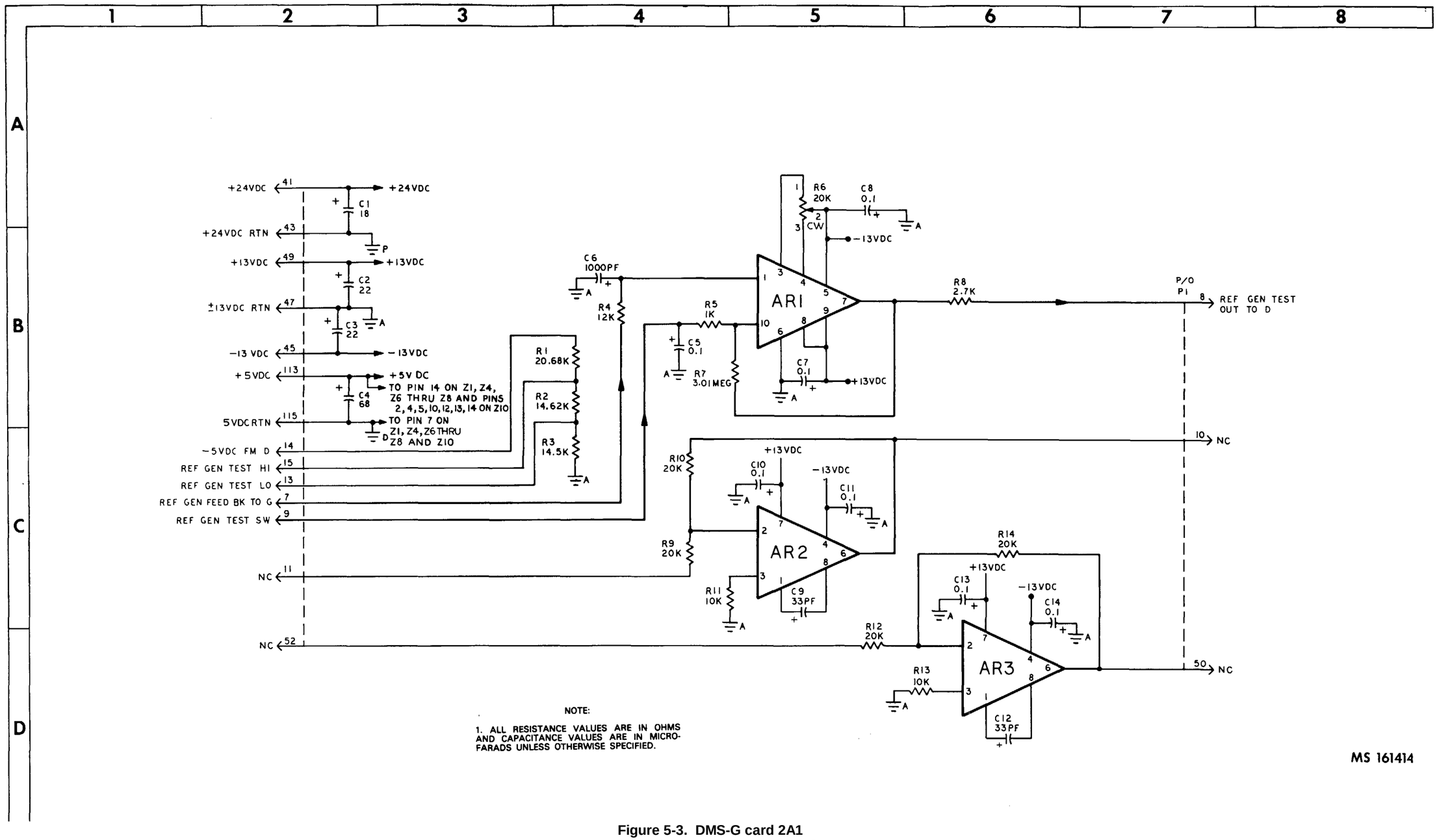


Figure 5-3. DMS-G card 2A1 schematic diagram (sheet 1 of 3)

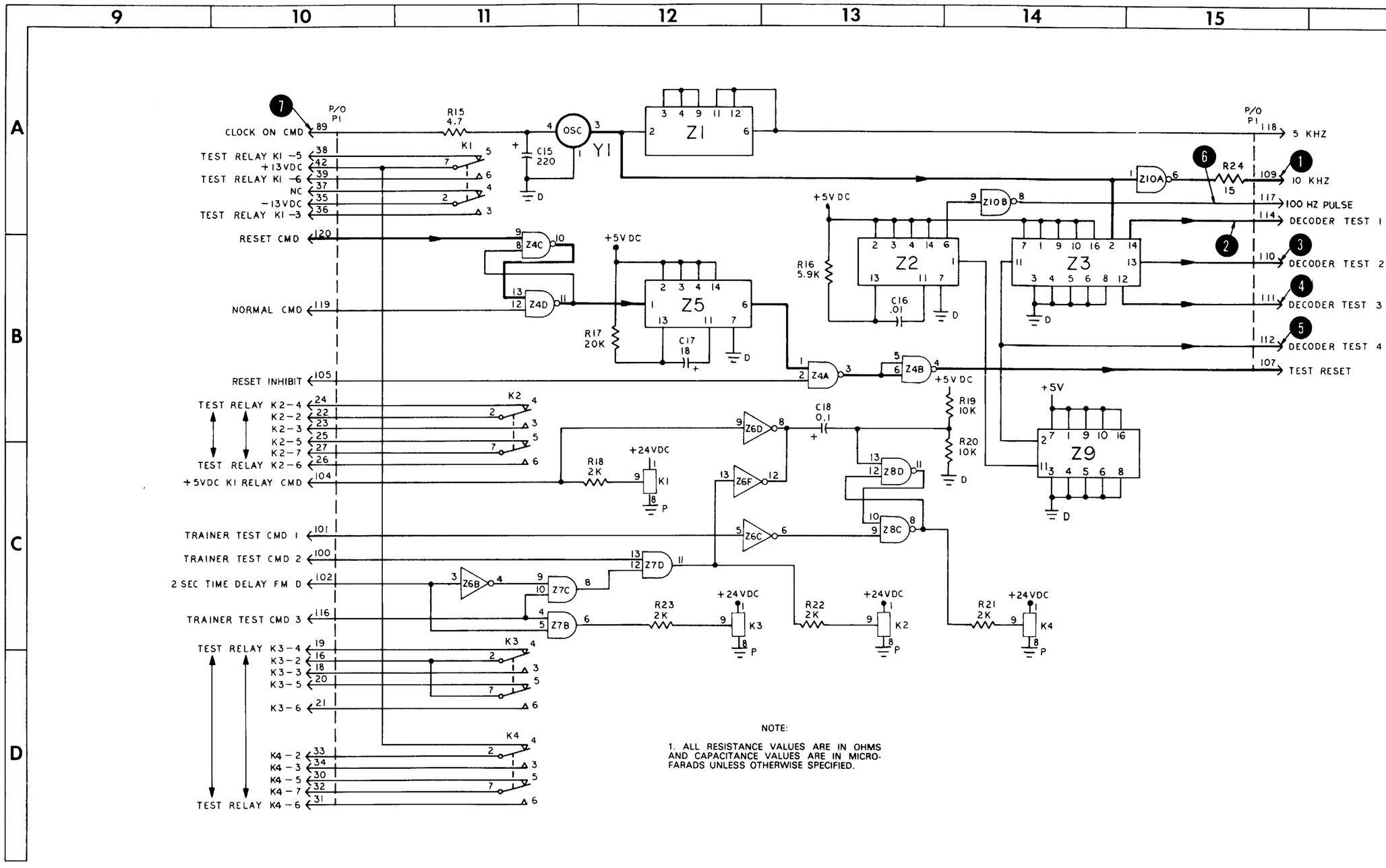
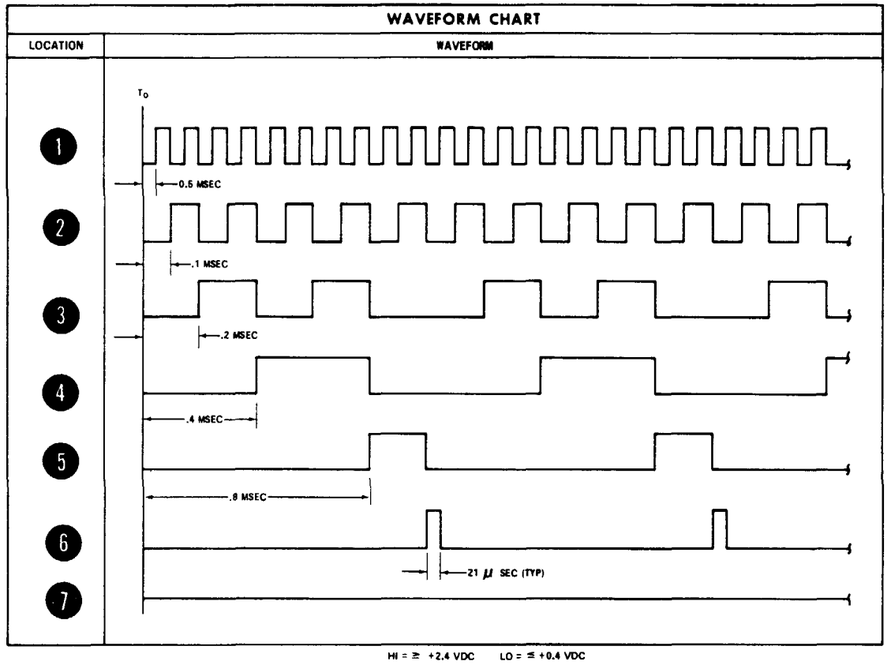


Figure 5-3. DMS-G card 2A1 schematic diagram (sheet 2 of 3)



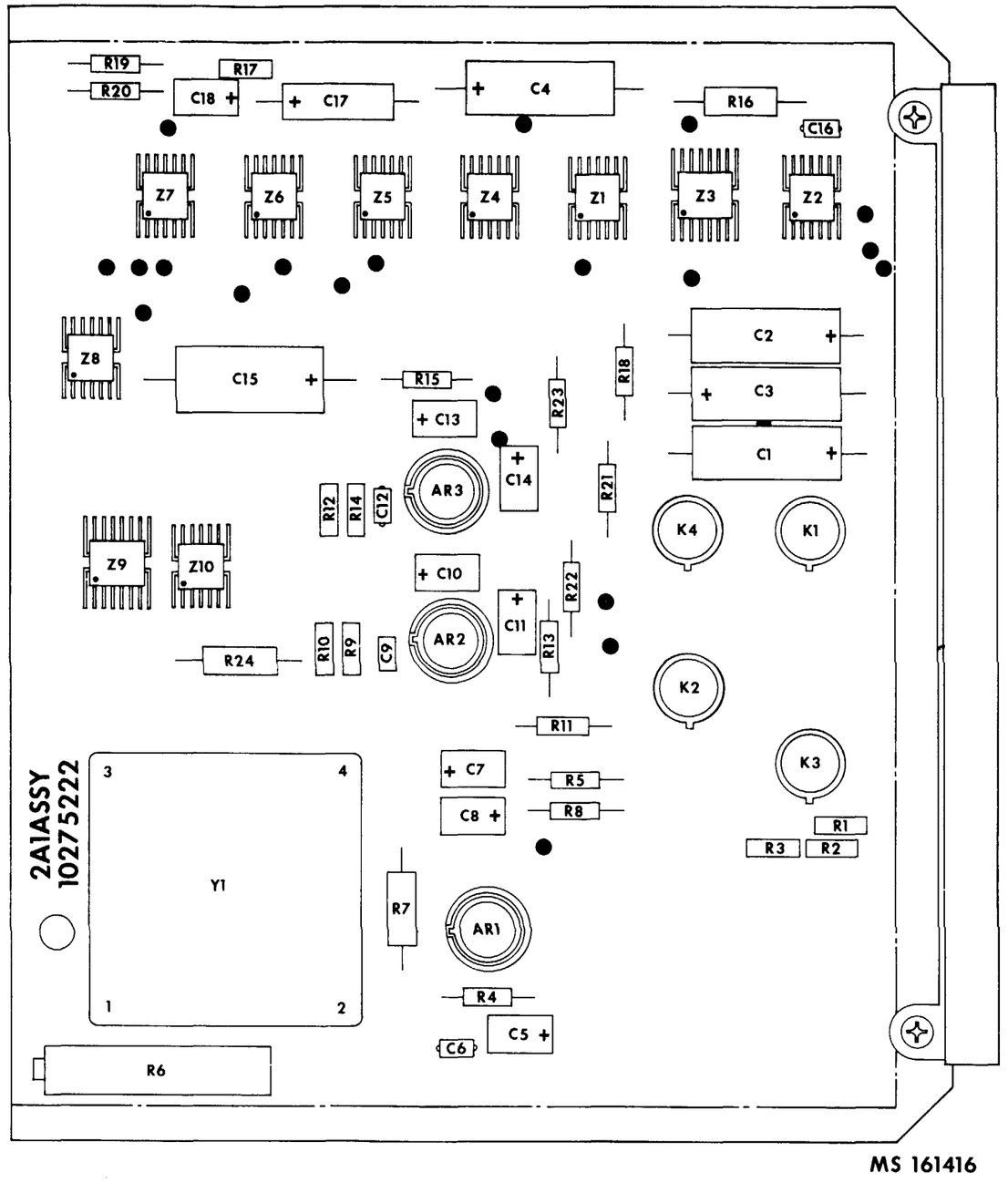


Figure 5-3. DMS-G card 2A1 (10275222) - schematic diagram (sheet 3 of 3)

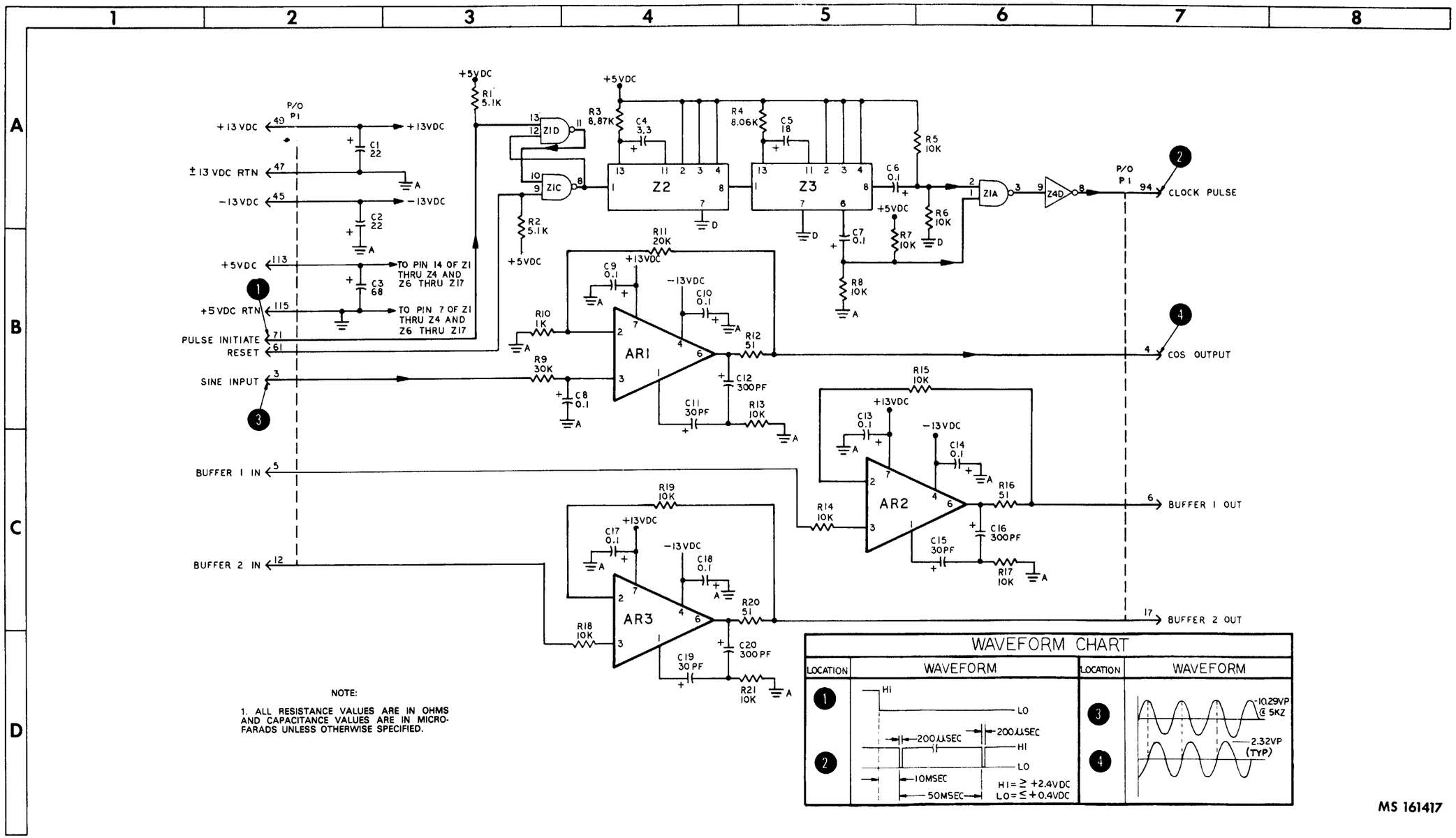
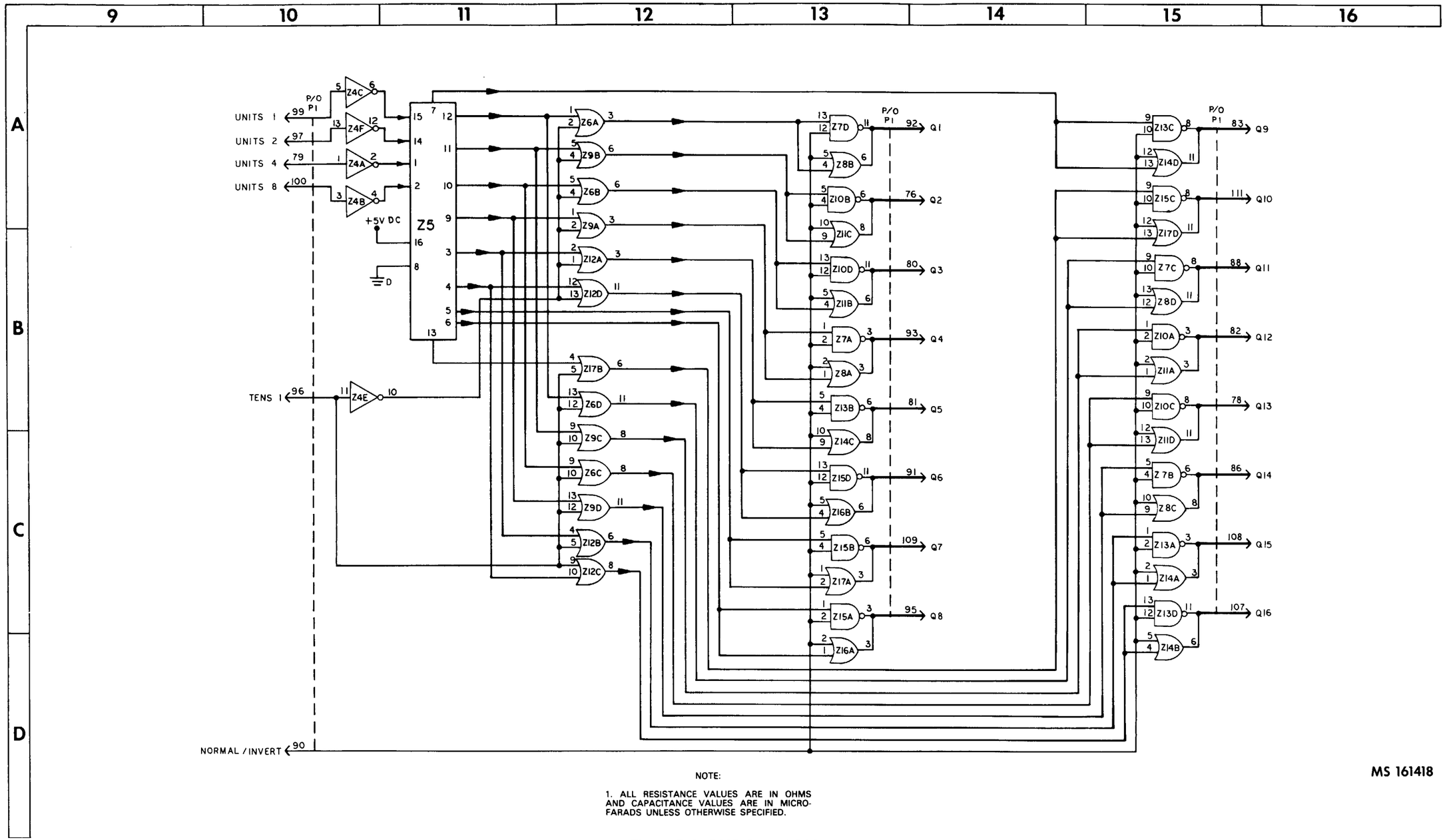


Figure 5-4. DMS-G card 2A2 schematic diagram (sheet 1 of 3)



NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

MS 161418

Figure 5-4. DMS-G card 2A2 schematic diagram (sheet 2 of 3)

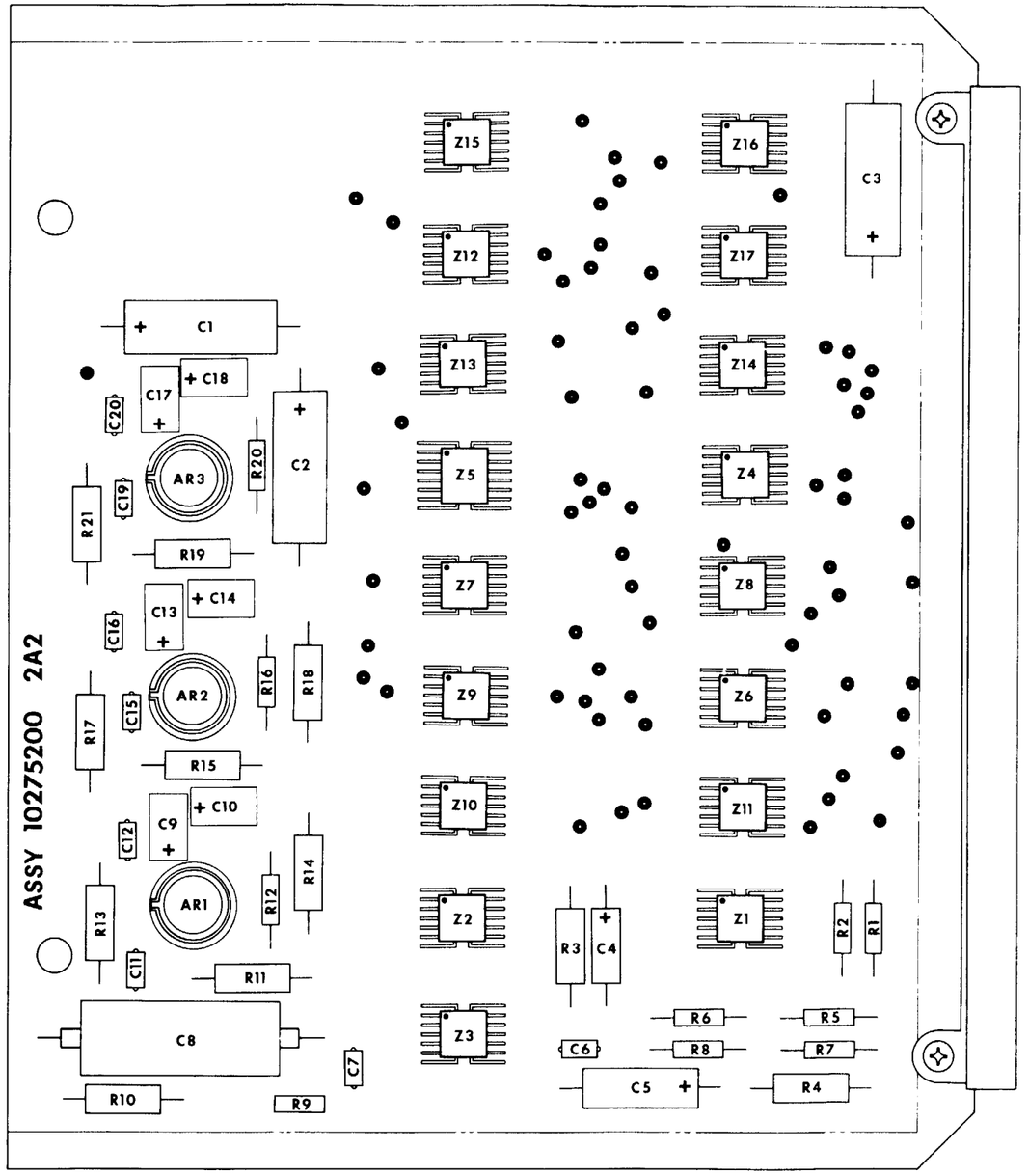


Figure 5-4. DMS-G card 2A2 (10275200) - schematic diagram (sheet 3 of 3)

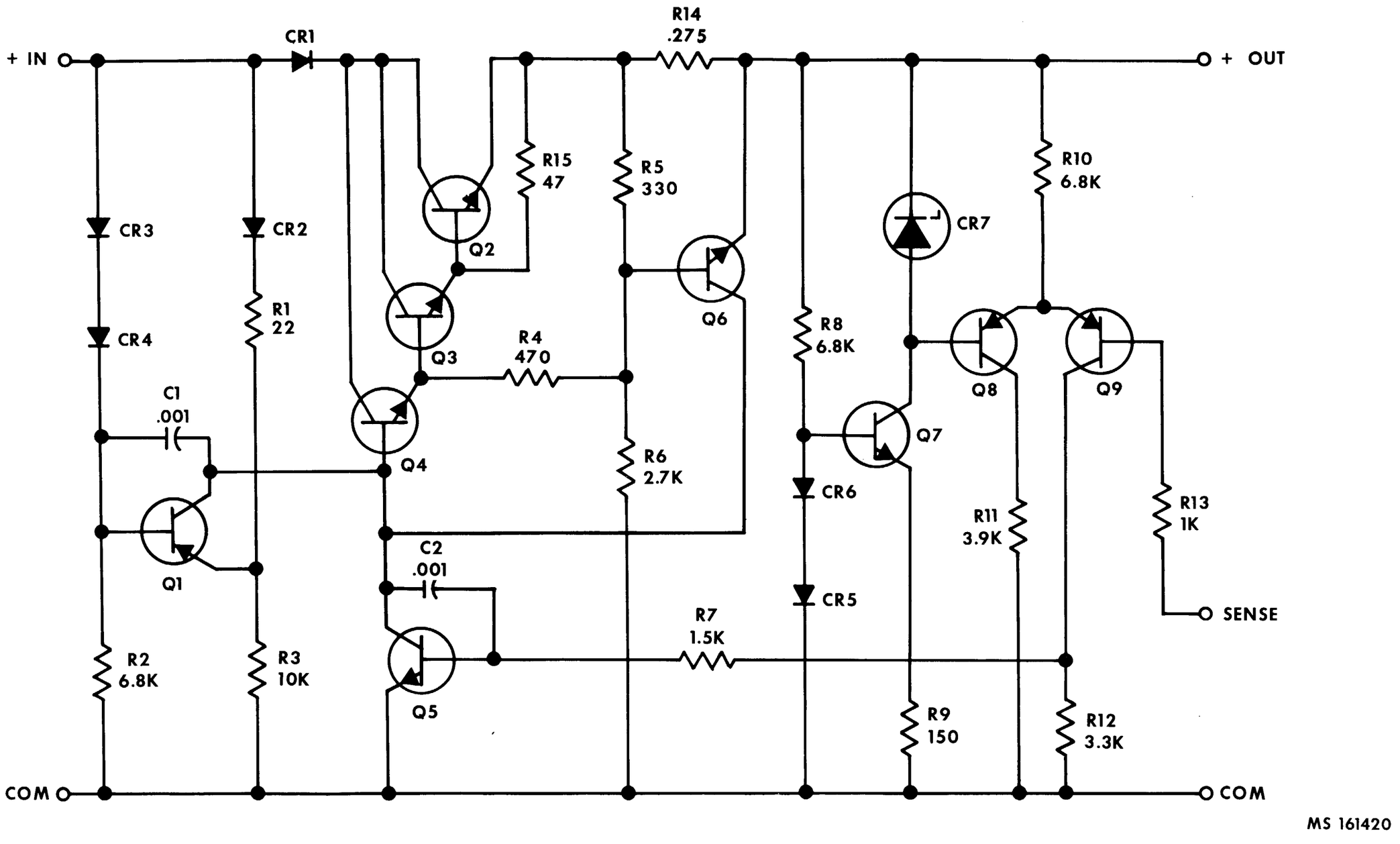


Figure 5-5. Positive Voltage Regulator (10275398-2) - schematic diagram

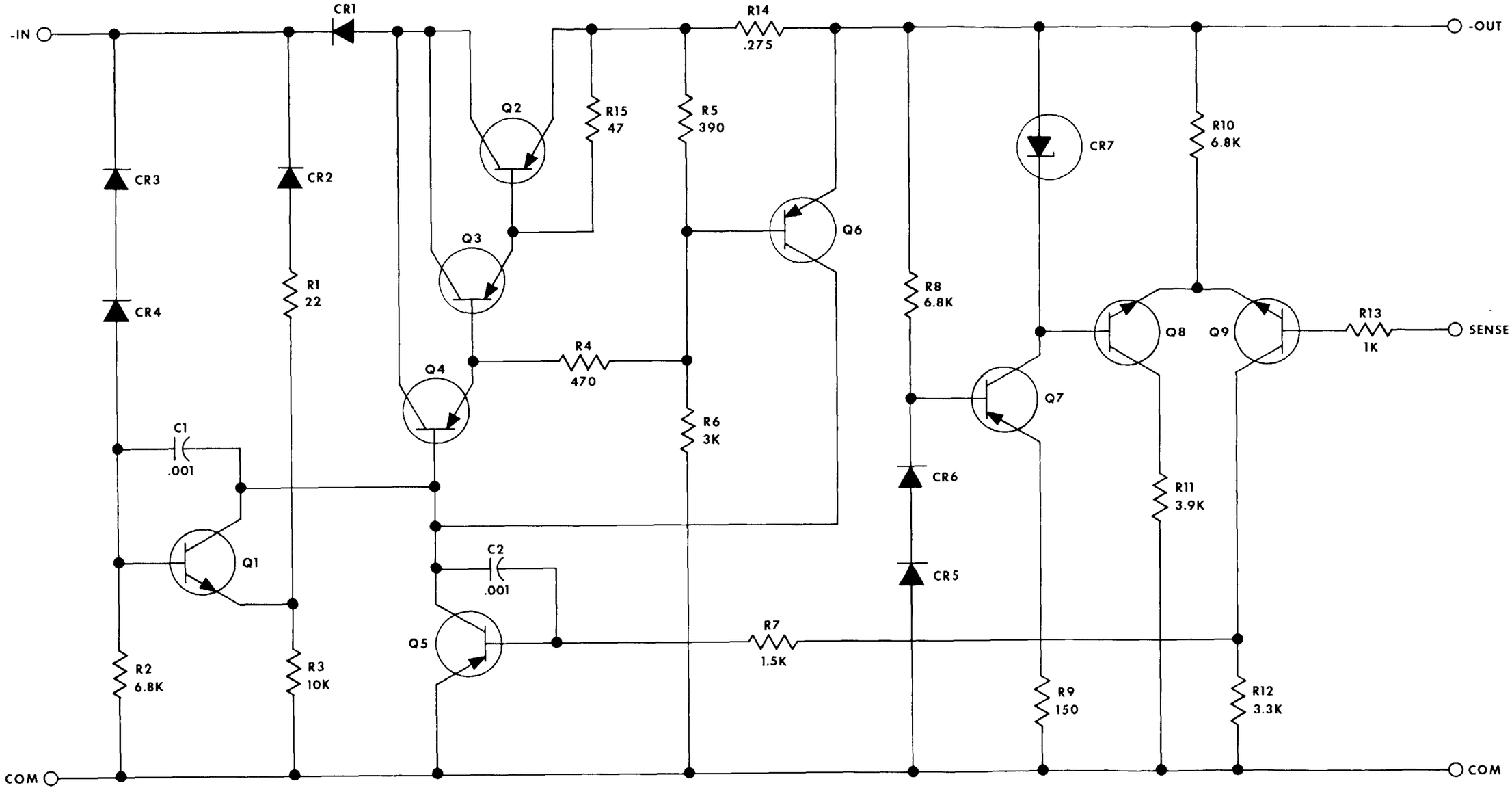
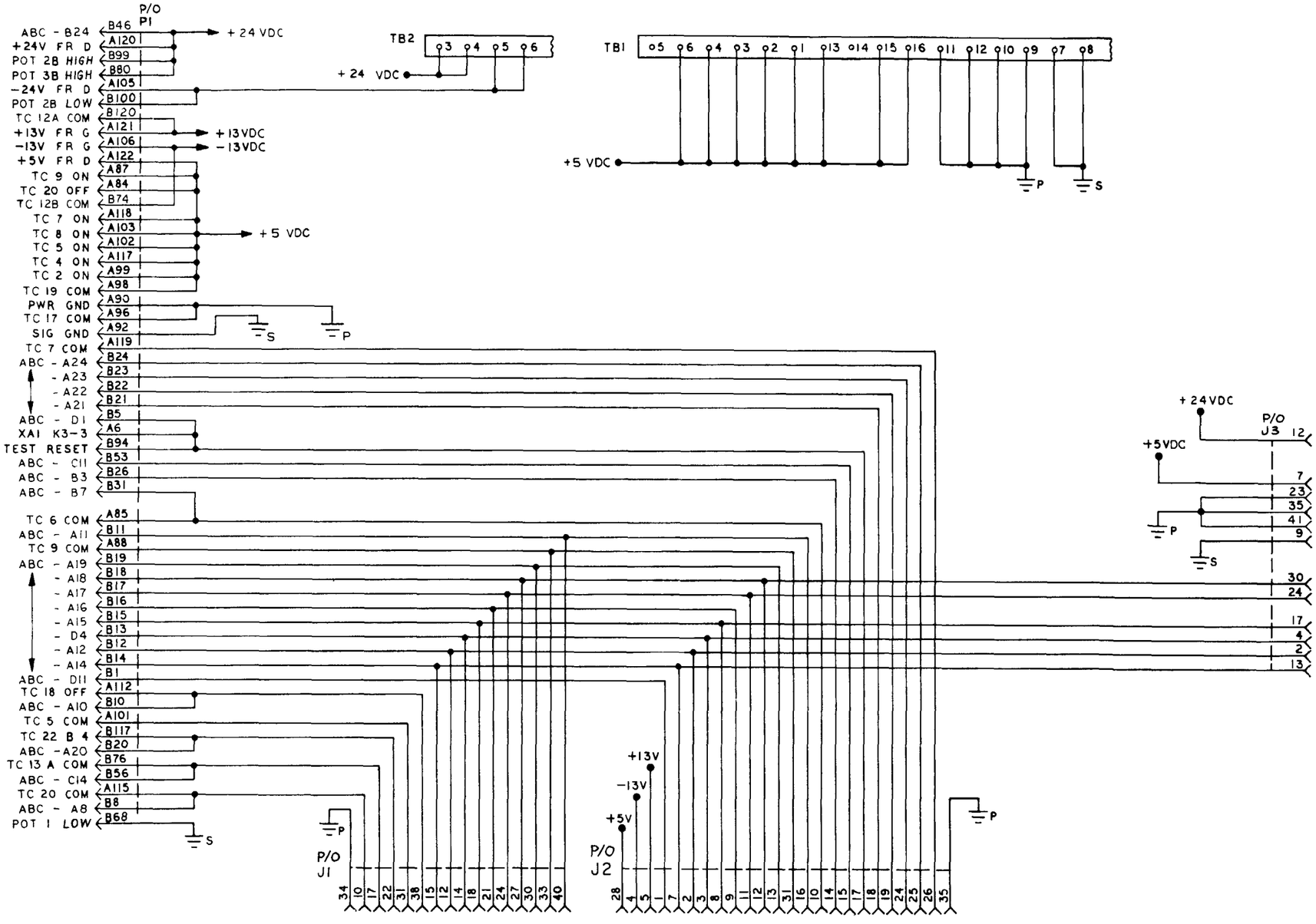
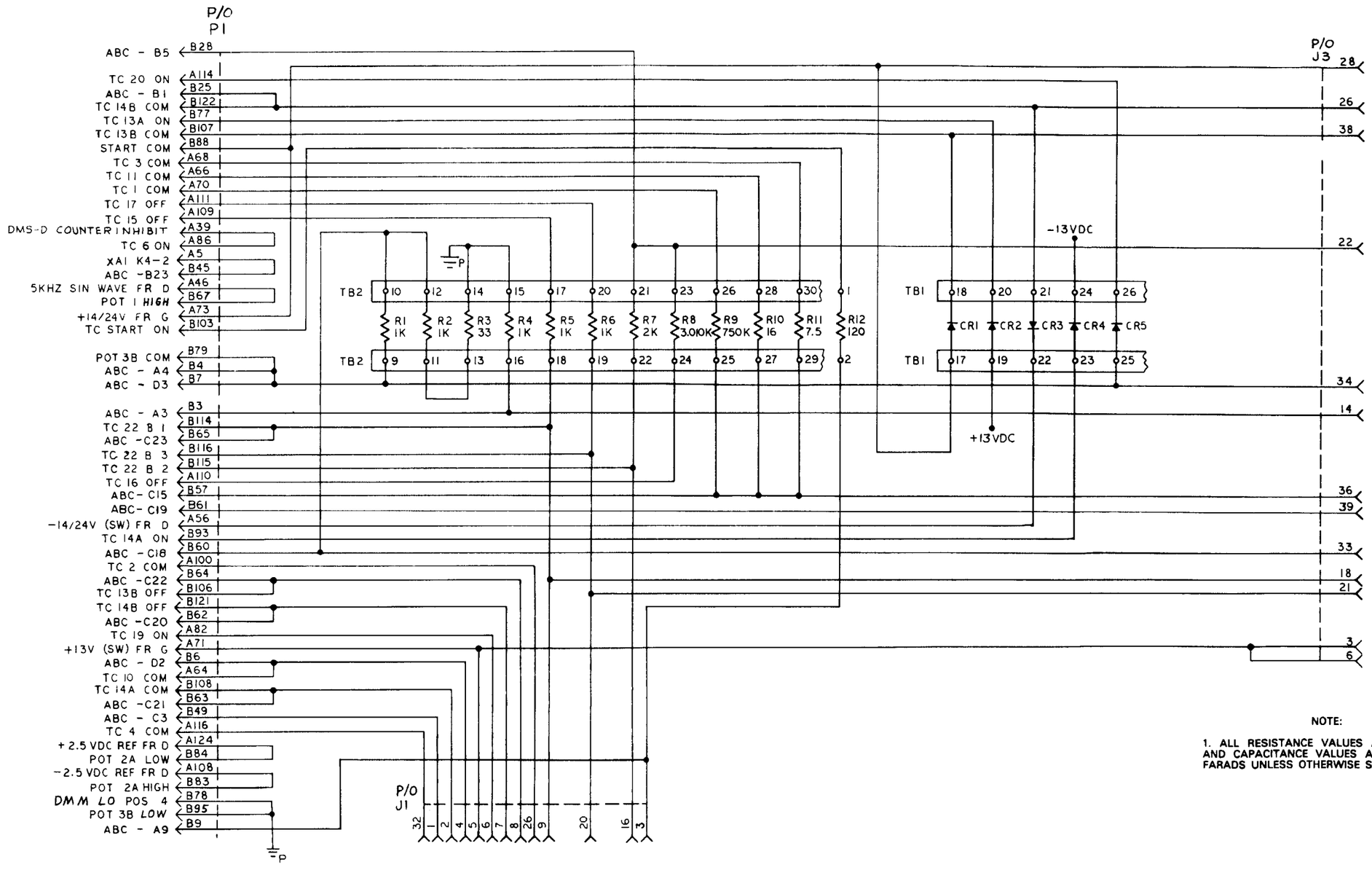


Figure 5-6. Negative Voltage Regulator (10275398-4) - schematic diagram



MS 161294

Figure 5-7. DMS-G test adapter A1 schematic diagram (sheet 1 of 3)

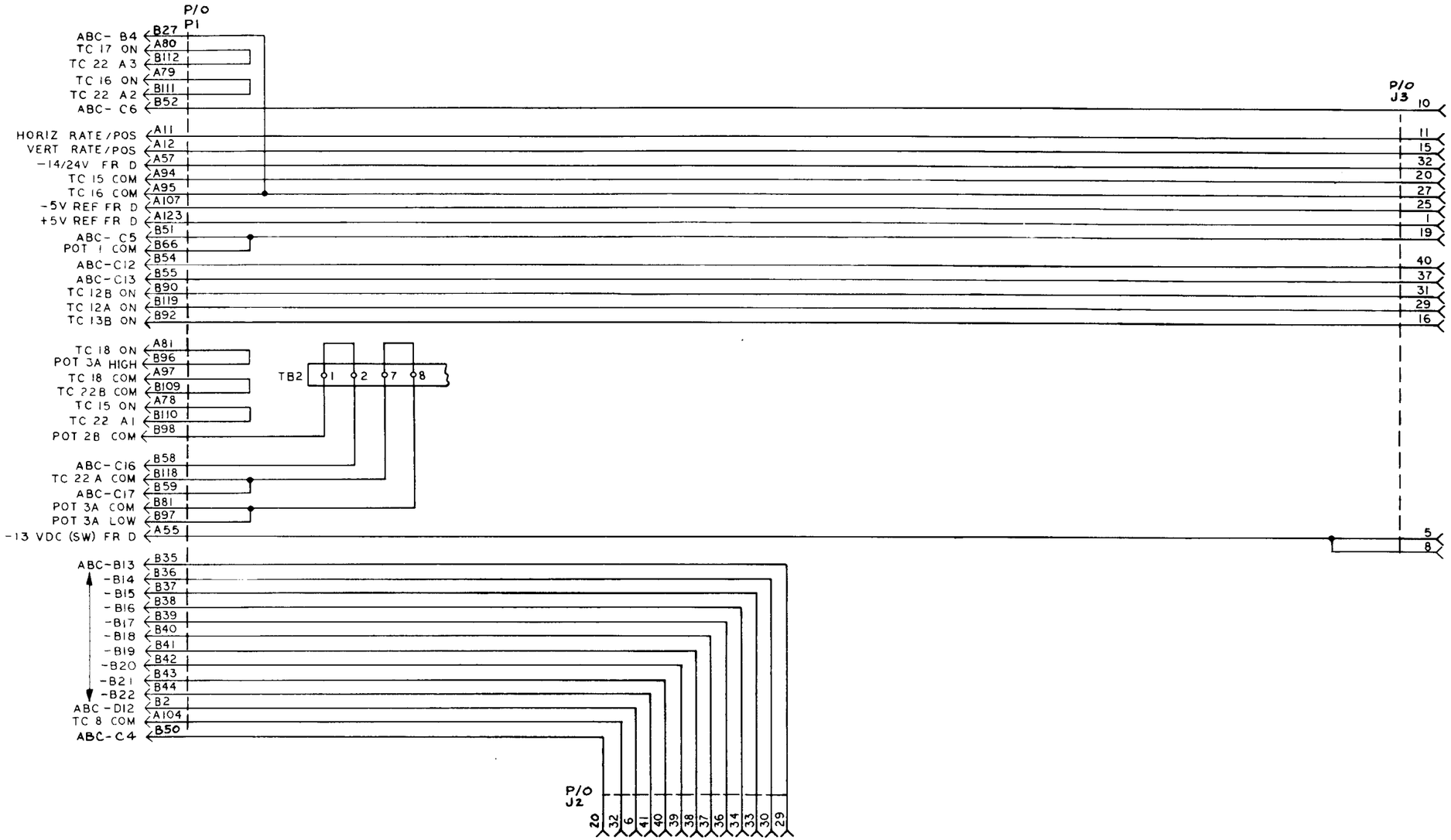


NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

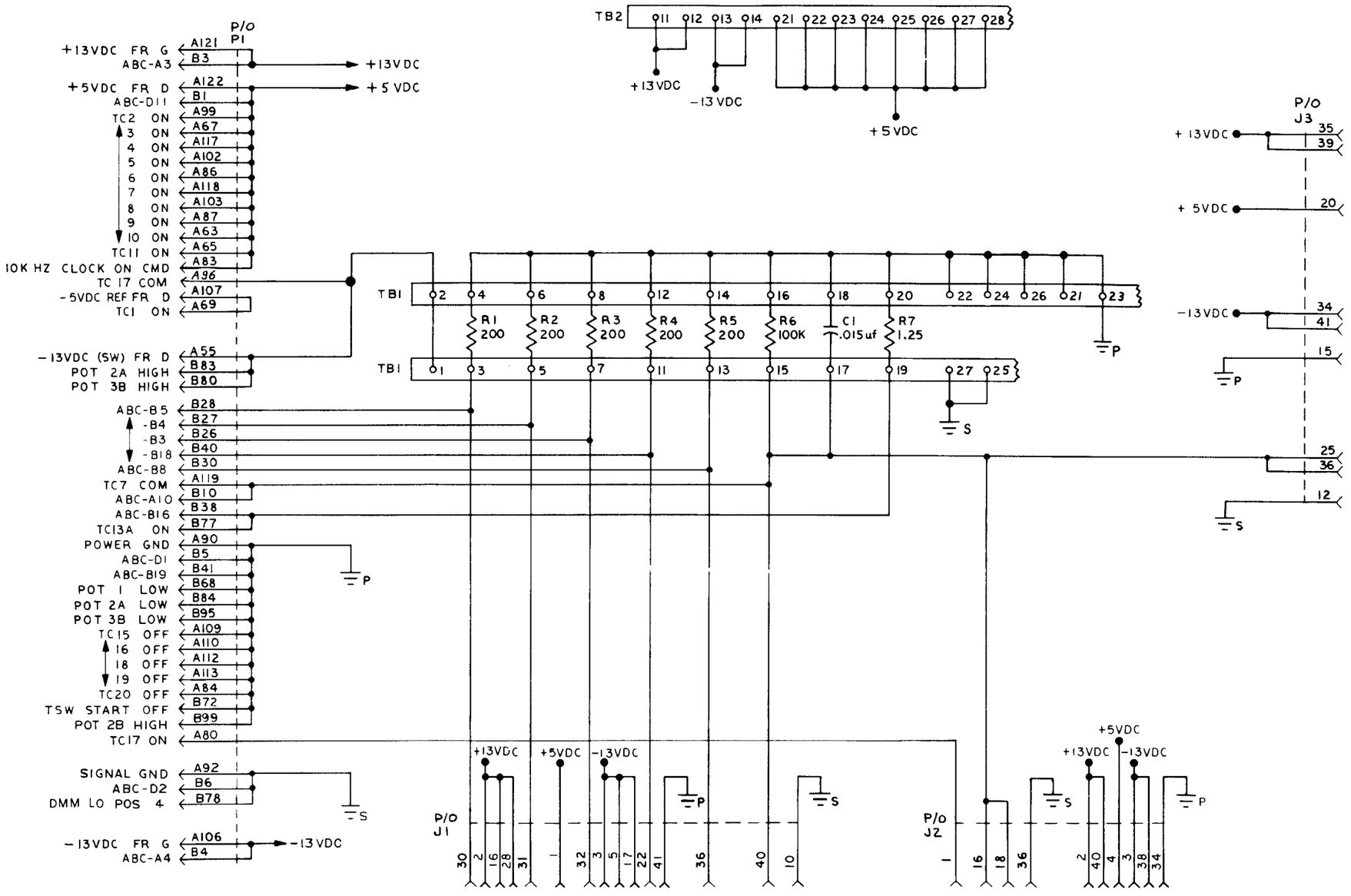
MS 161295

Figure 5-7. DMS-G test adapter A1 schematic diagram (sheet 2 of 3)



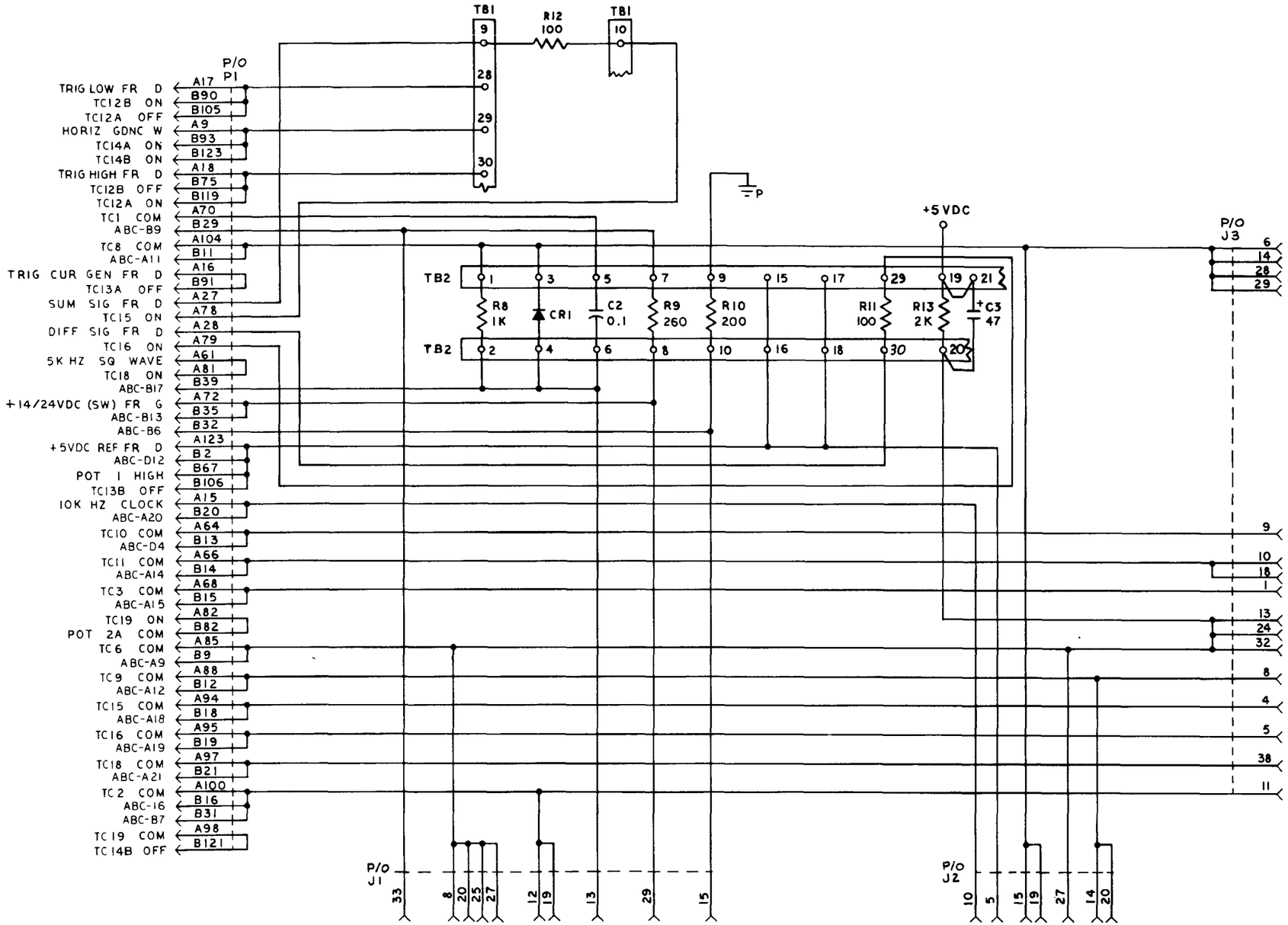
MS 161296

Figure 5-7. DMS-G test adapter AI (10275268) - schematic diagram (sheet 3 of 3)



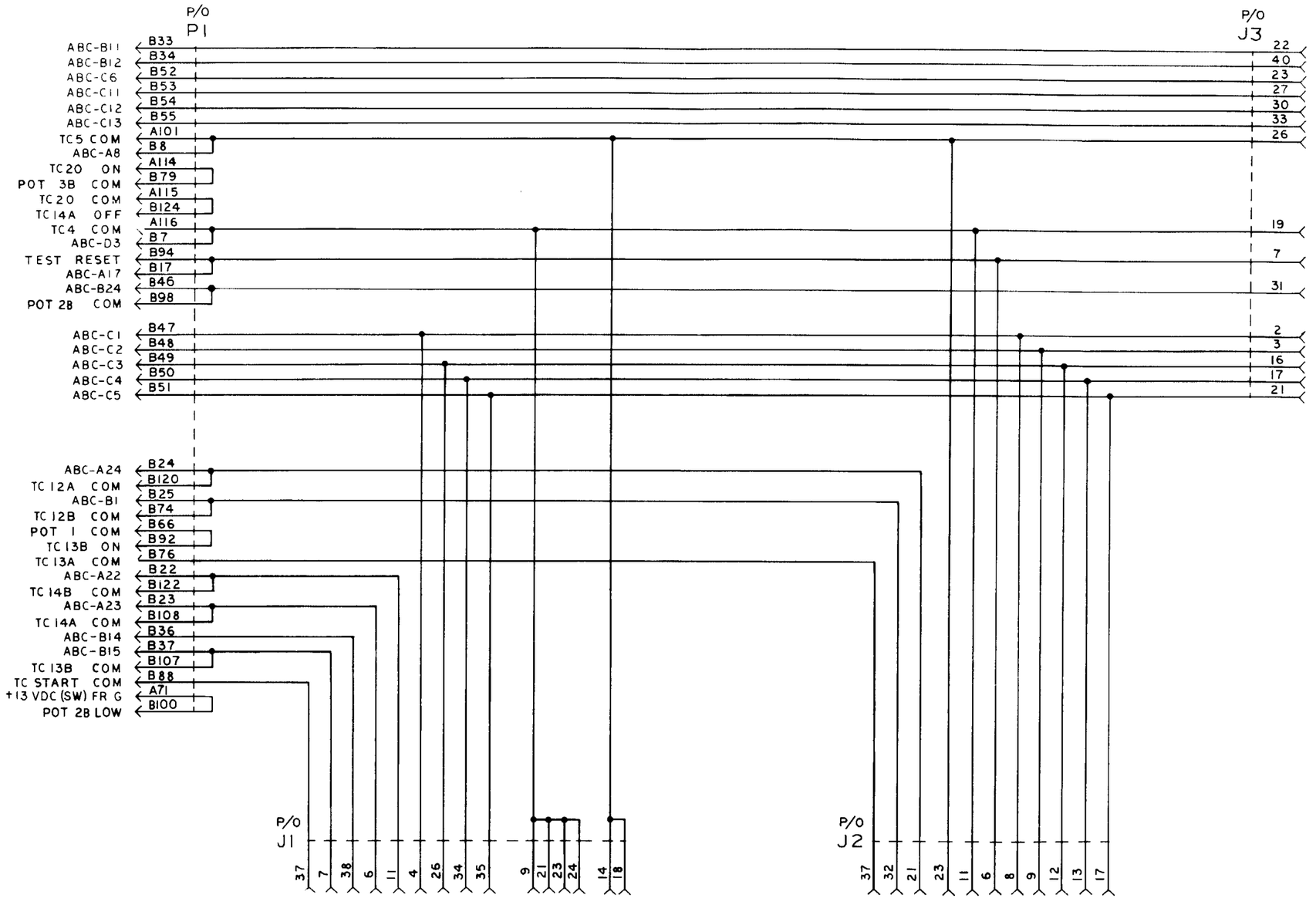
MS 161297

Figure 5-8. DMS-G test adapter A2 (10275269) - schematic diagram (sheet 1 of 3)



MS 161298

Figure 5-8. DMS-G test adapter A2 (10275269) - schematic diagram (sheet 2 of 3)



MS 161299

Figure 5-8. DMS-G test adapter A2 (10275269) - schematic diagram (sheet 3 of 3)

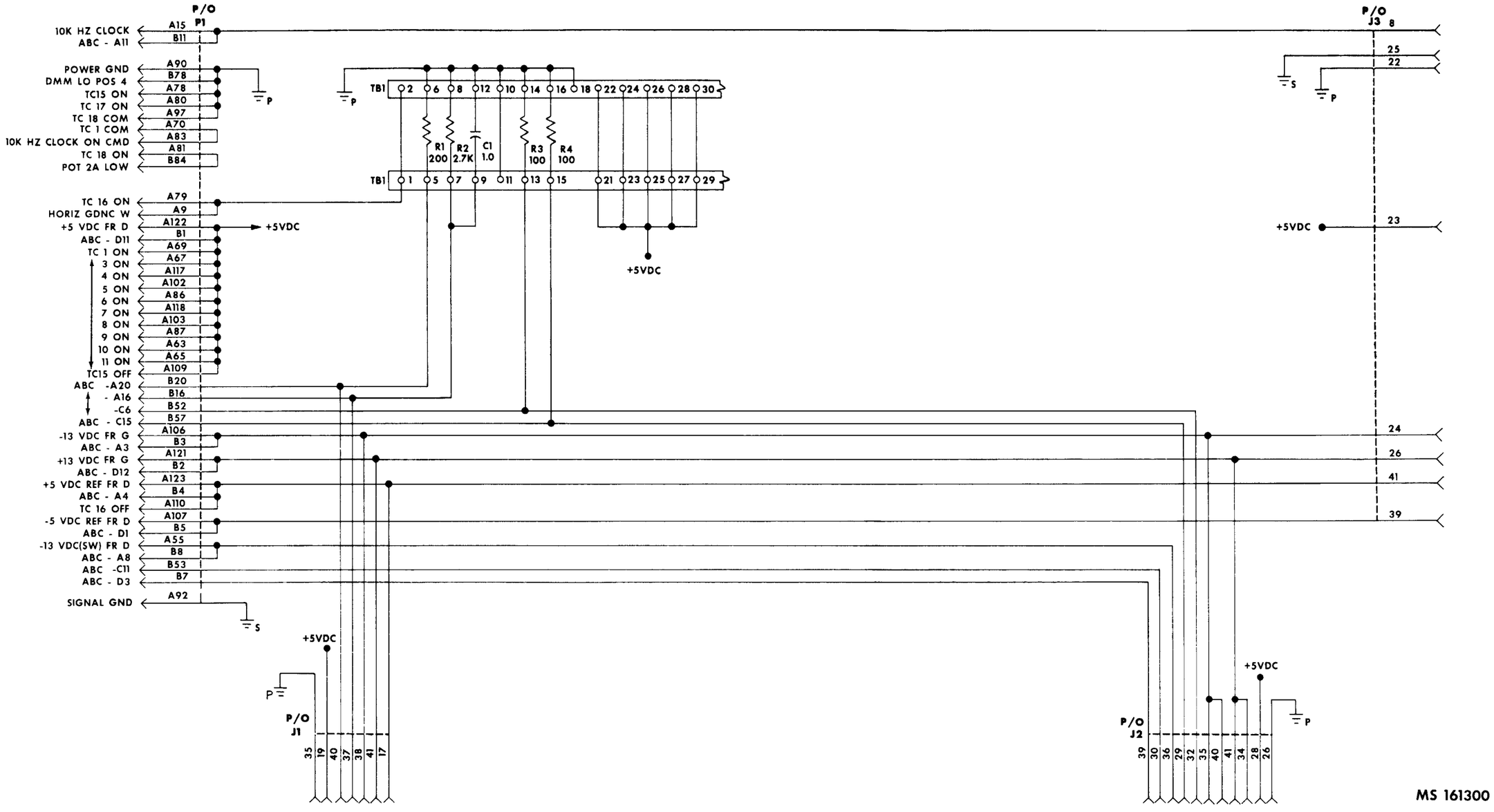


Figure 5-9. DMS-G test adapter A3 (10275270) - schematic diagram (sheet 1 of 2)

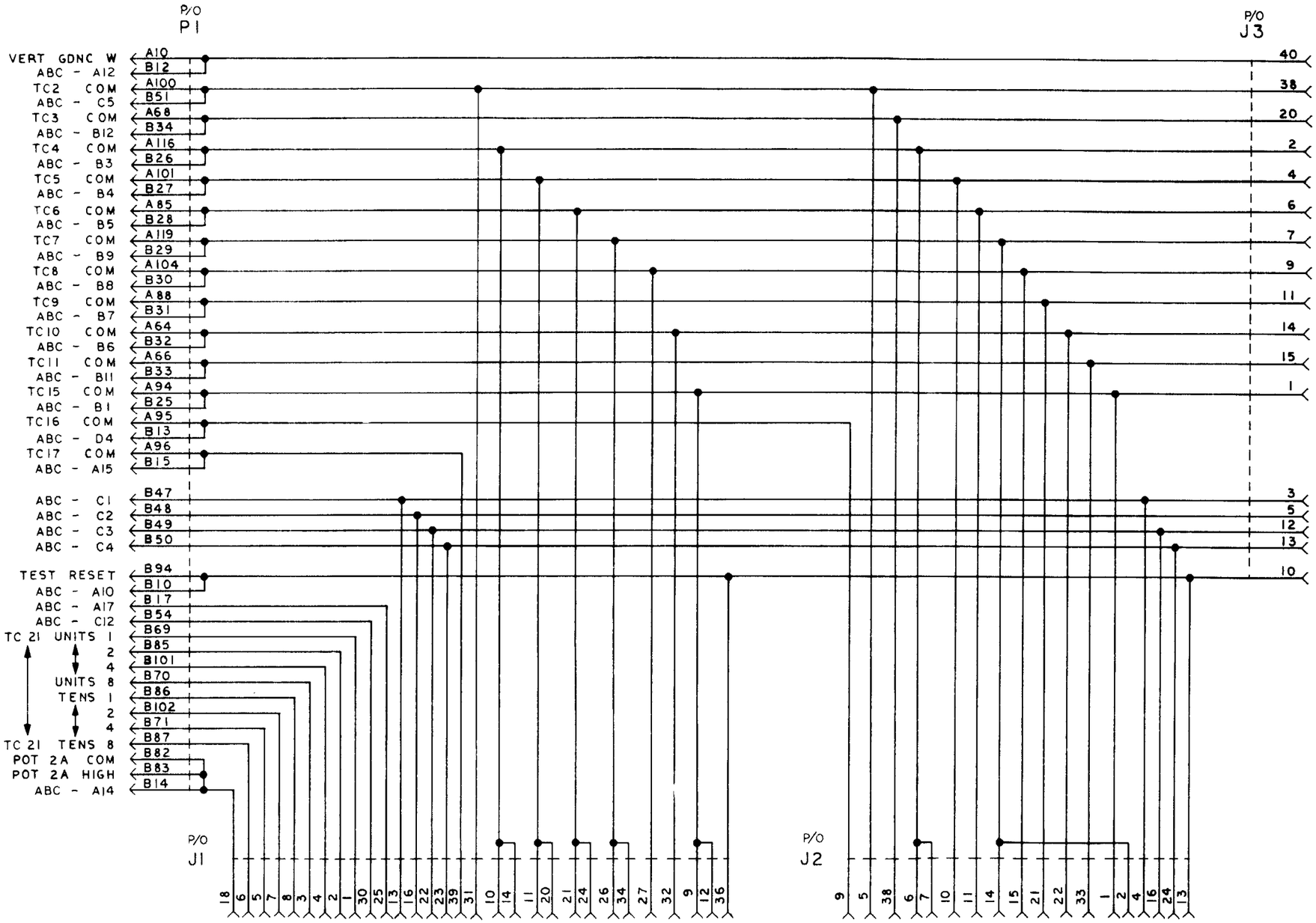
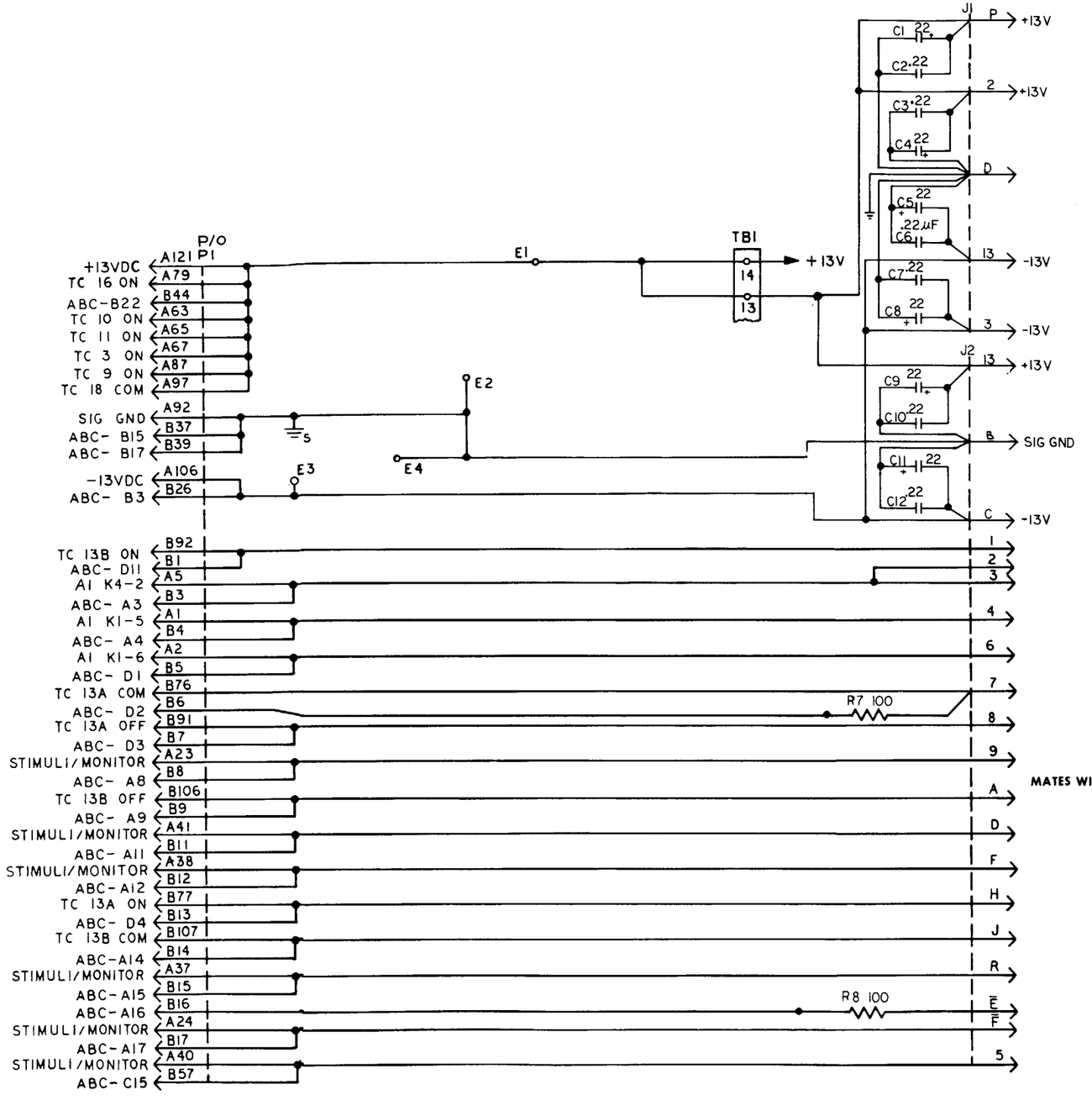


Figure 5-9. DMS-G test adapter A3 (10275270) - schematic diagram (sheet 2 of 2)



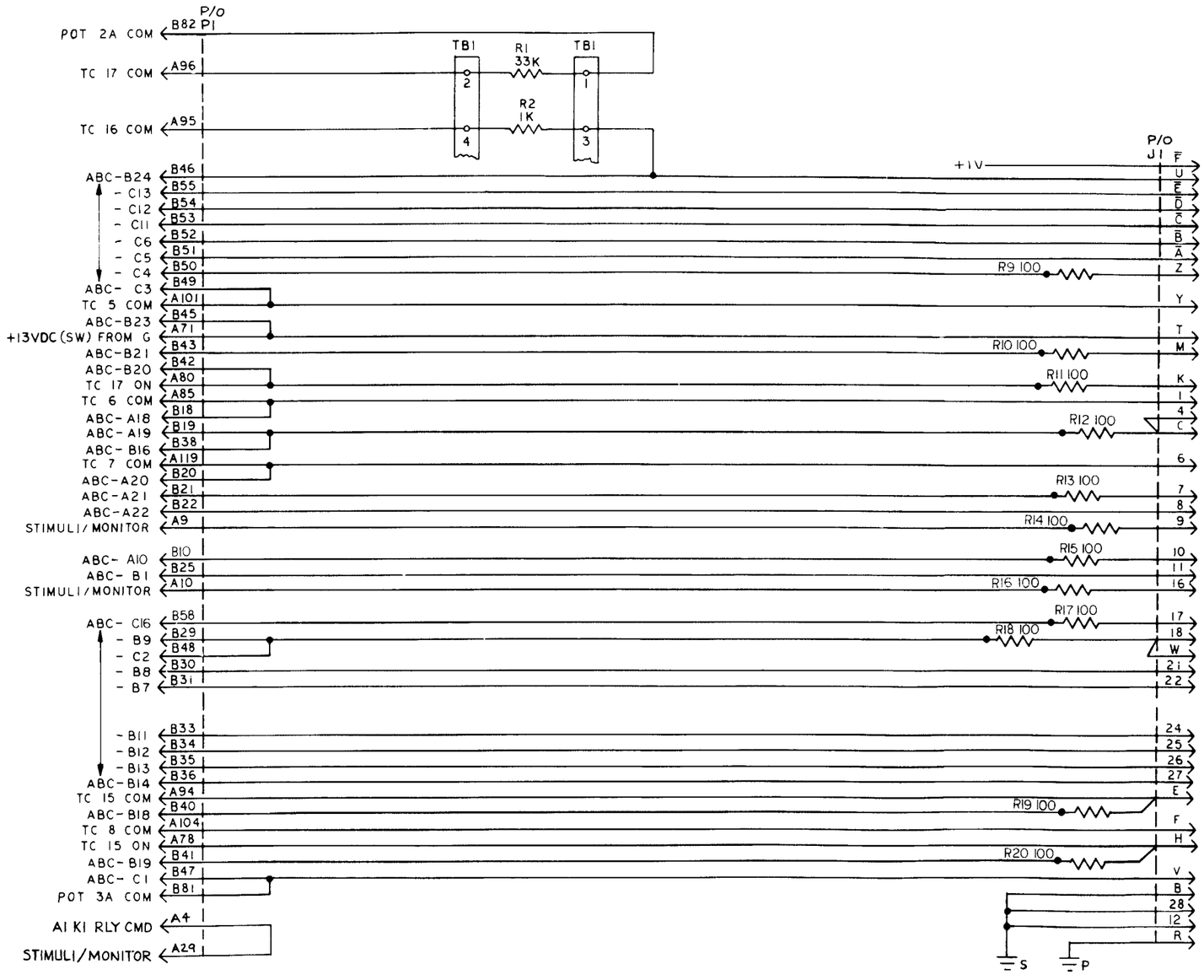
NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

MATES WITH MTS CARD A2

MS 161302

Figure 5-10. DMS-G test adapter A4 schematic diagram (sheet 1 of 3)



MATES WITH MTS CARD A1

NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

MS 161303

Figure 5-10. DMS-G test adapter A4 schematic diagram (sheet 2 of 3)

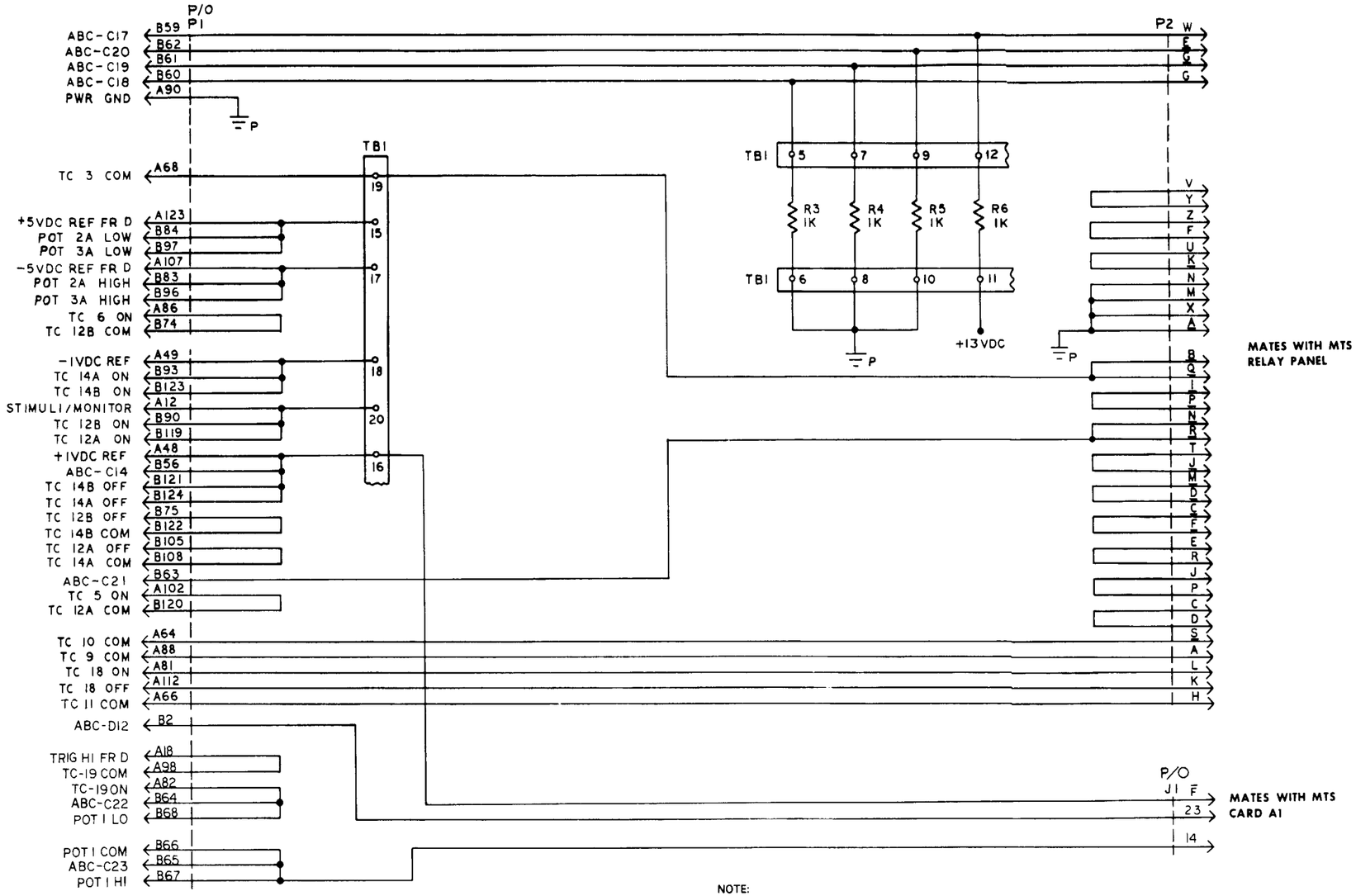
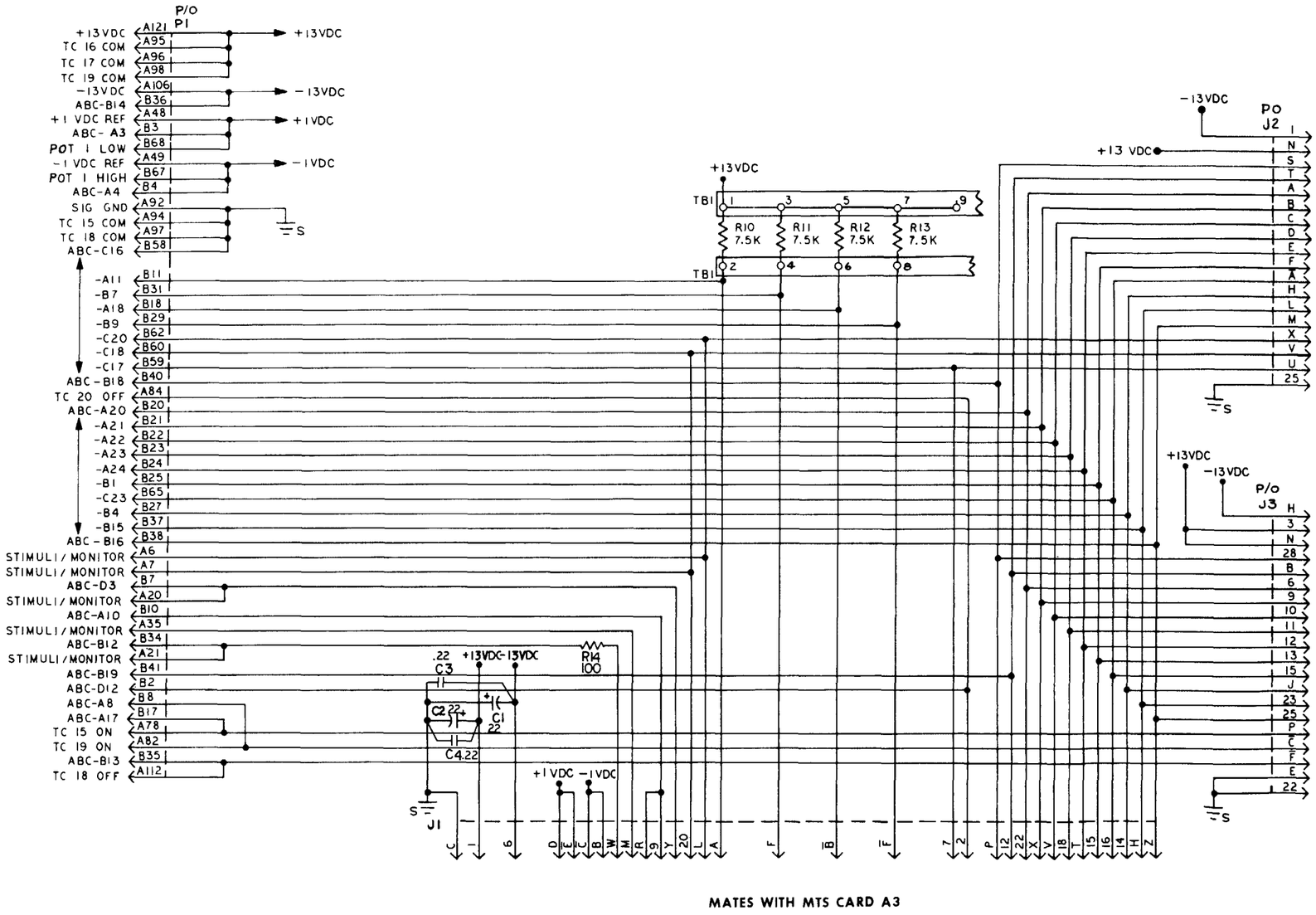


Figure 5-10. DMS-G test adapter A4 schematic diagram (sheet 3 of 3)

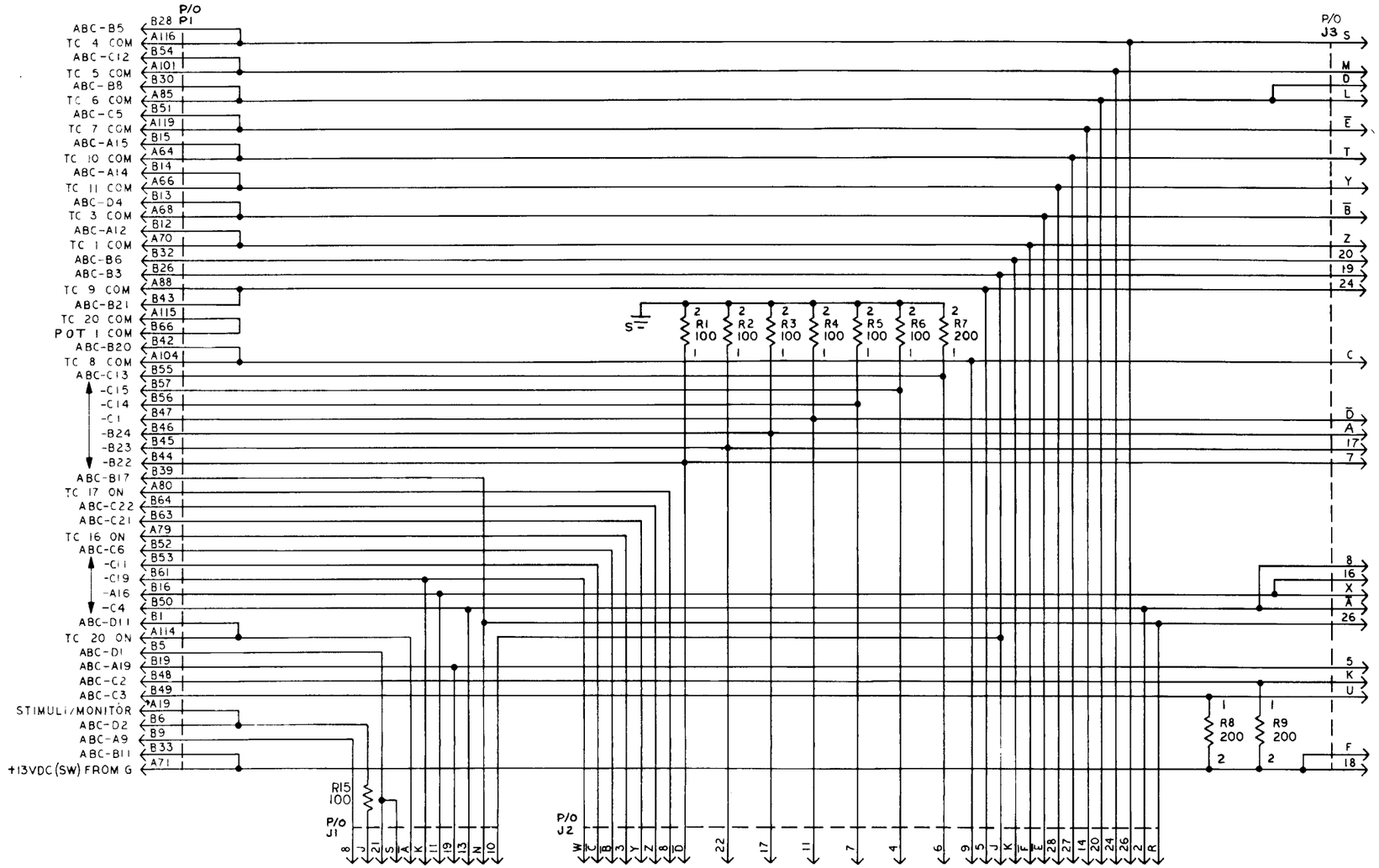


NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

MS 161305

Figure 5-11. DMS-G test adapter A5 schematic diagram (sheet 1 of 2)

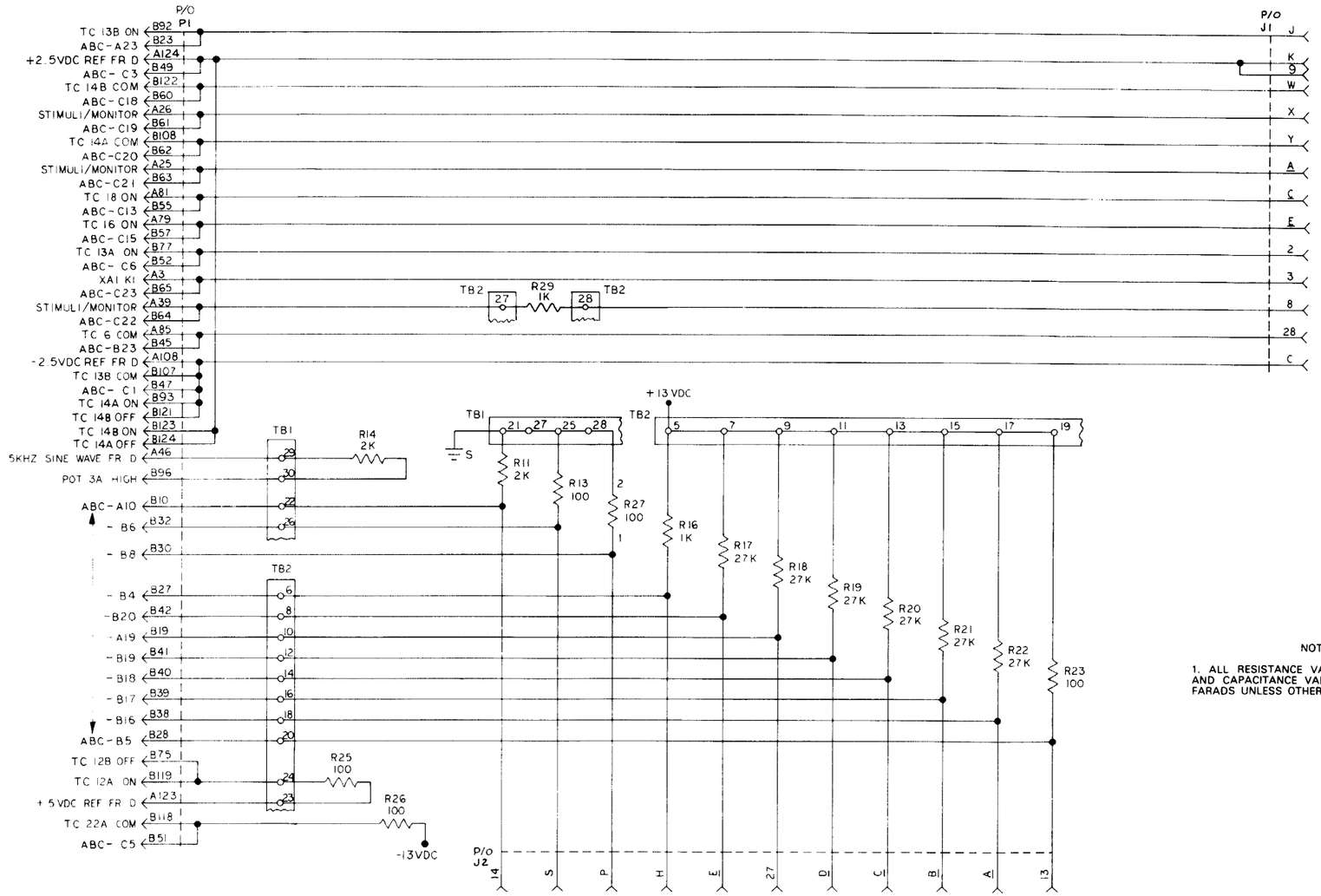


NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

MS 161306

Figure 5-11. DMS-G test adapter A5 schematic diagram (sheet 2 of 2)



NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

MS161307

Figure 5-12. DMS-G test adapter A6 schematic diagram (sheet 1 of 3)

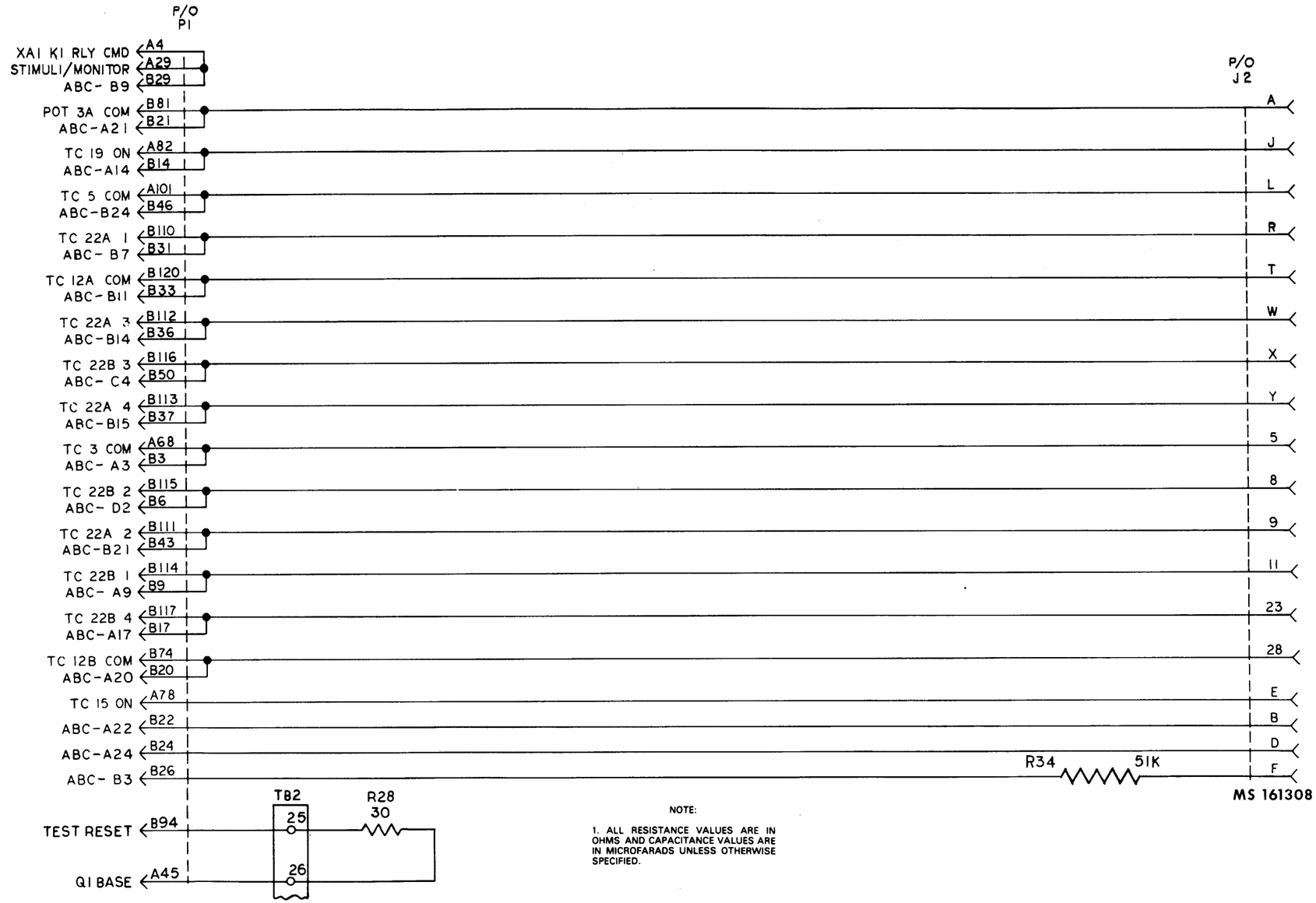
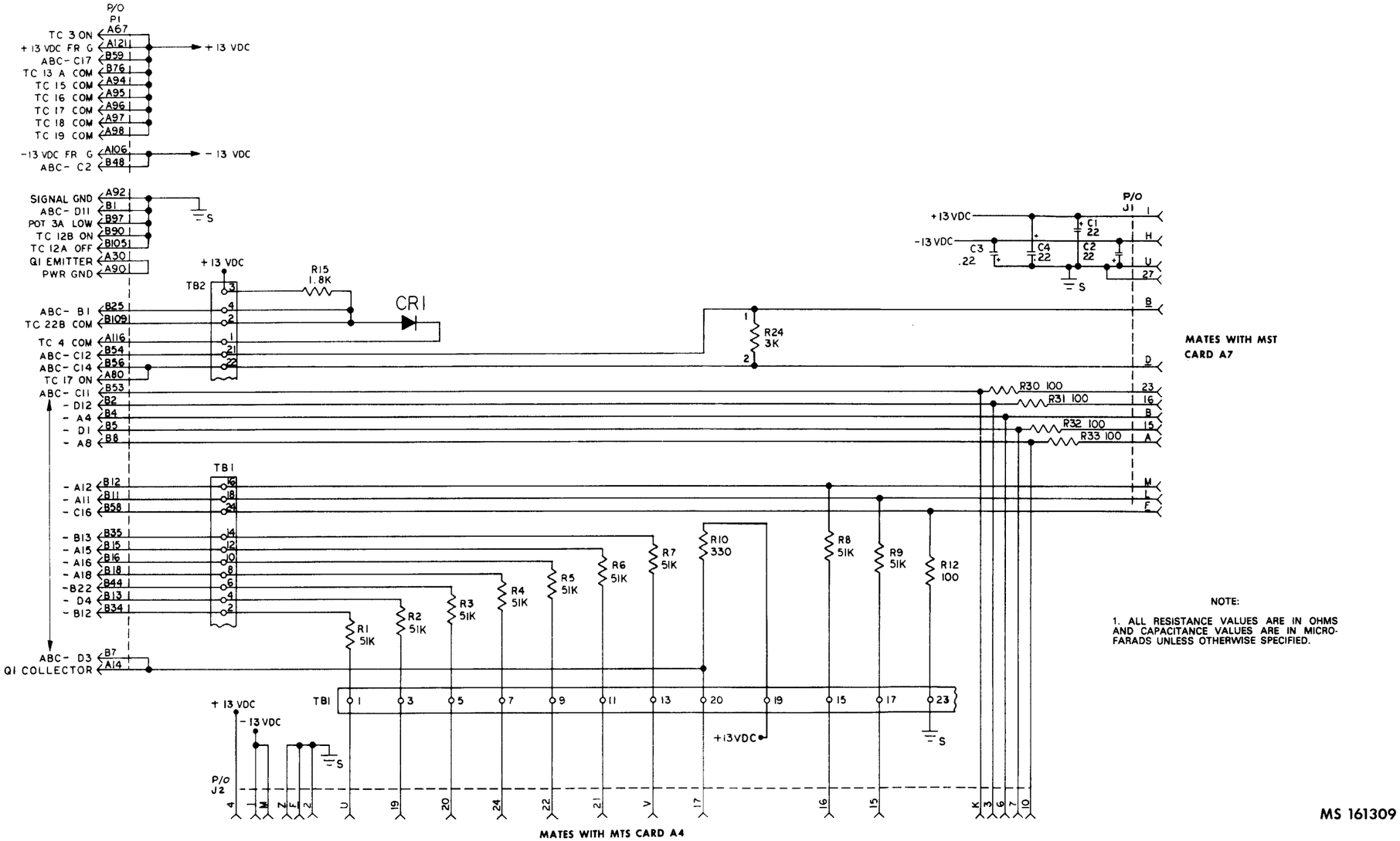


Figure 5-12. DMS-G TEST ADAPTER A6 schematic diagram (sheet 2 of 3)



NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

MS 161309

Figure 5-12. DMS-G test adapter A6 schematic diagram (sheet 3 of 3)

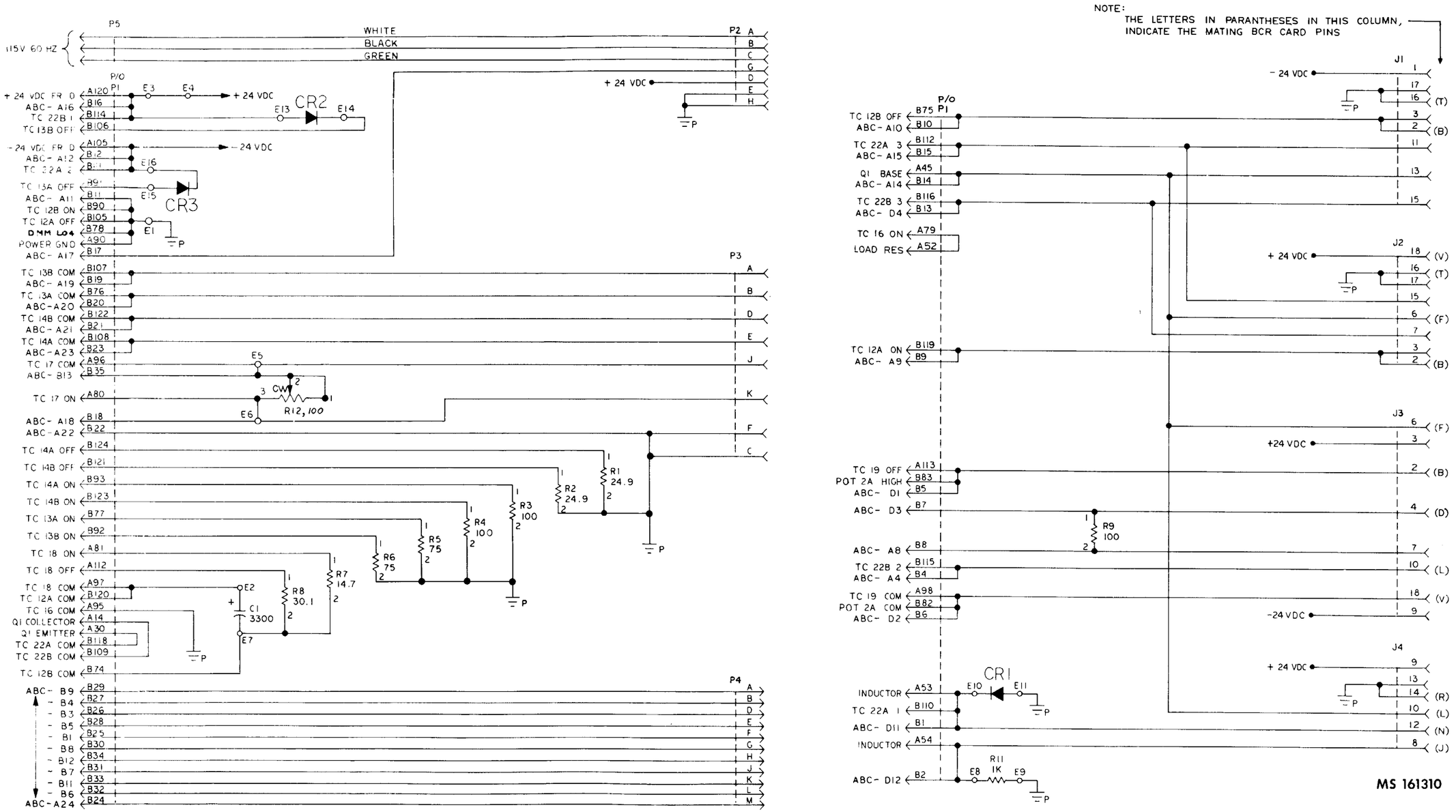
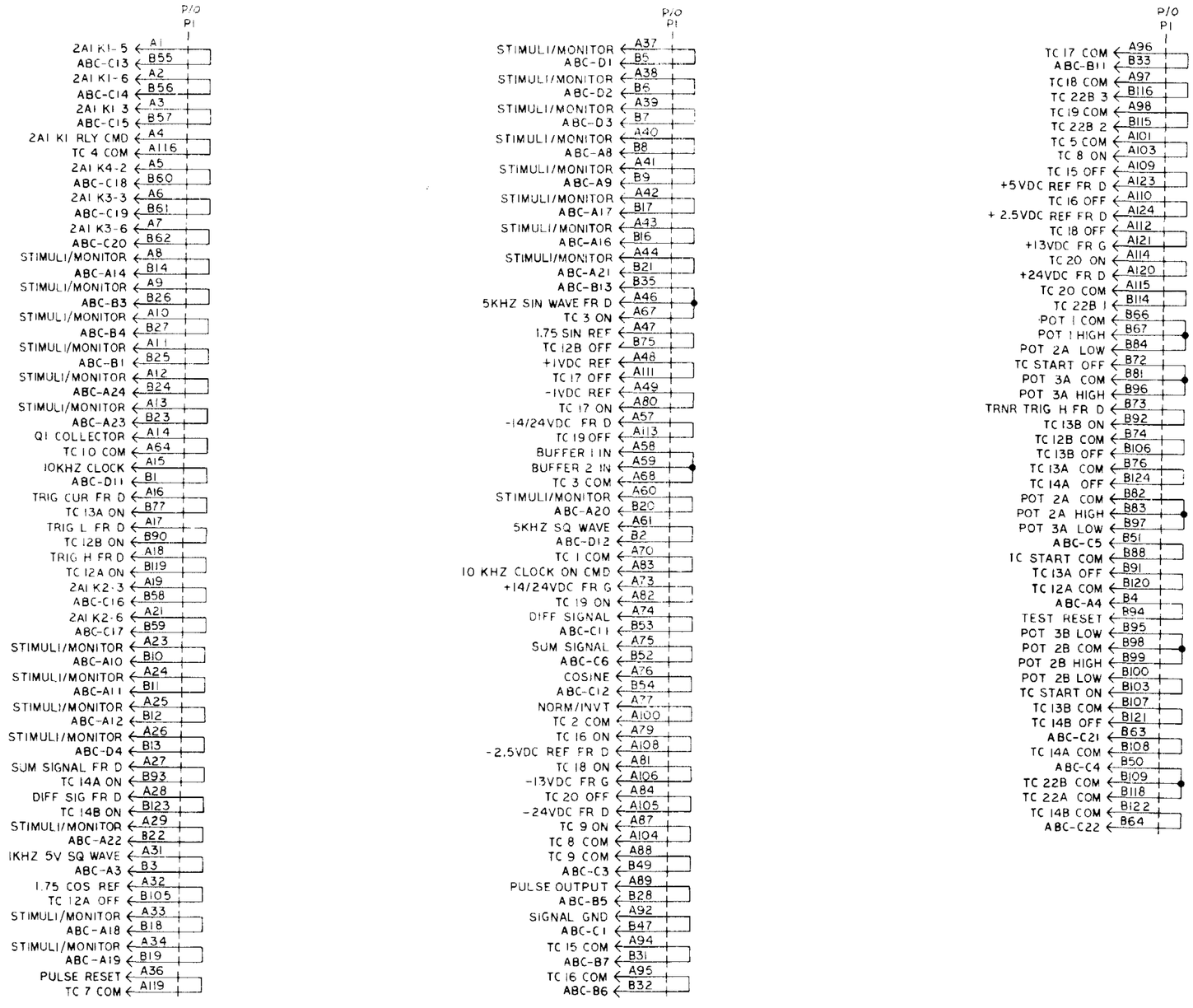


Figure 5-13. DMS-G test adapter A7 (10275274)-schematic diagram



MS 161311

Figure 5-14. DMS-G test adapter A8 (10275275)-schematic diagram (sheet 1 of 2)

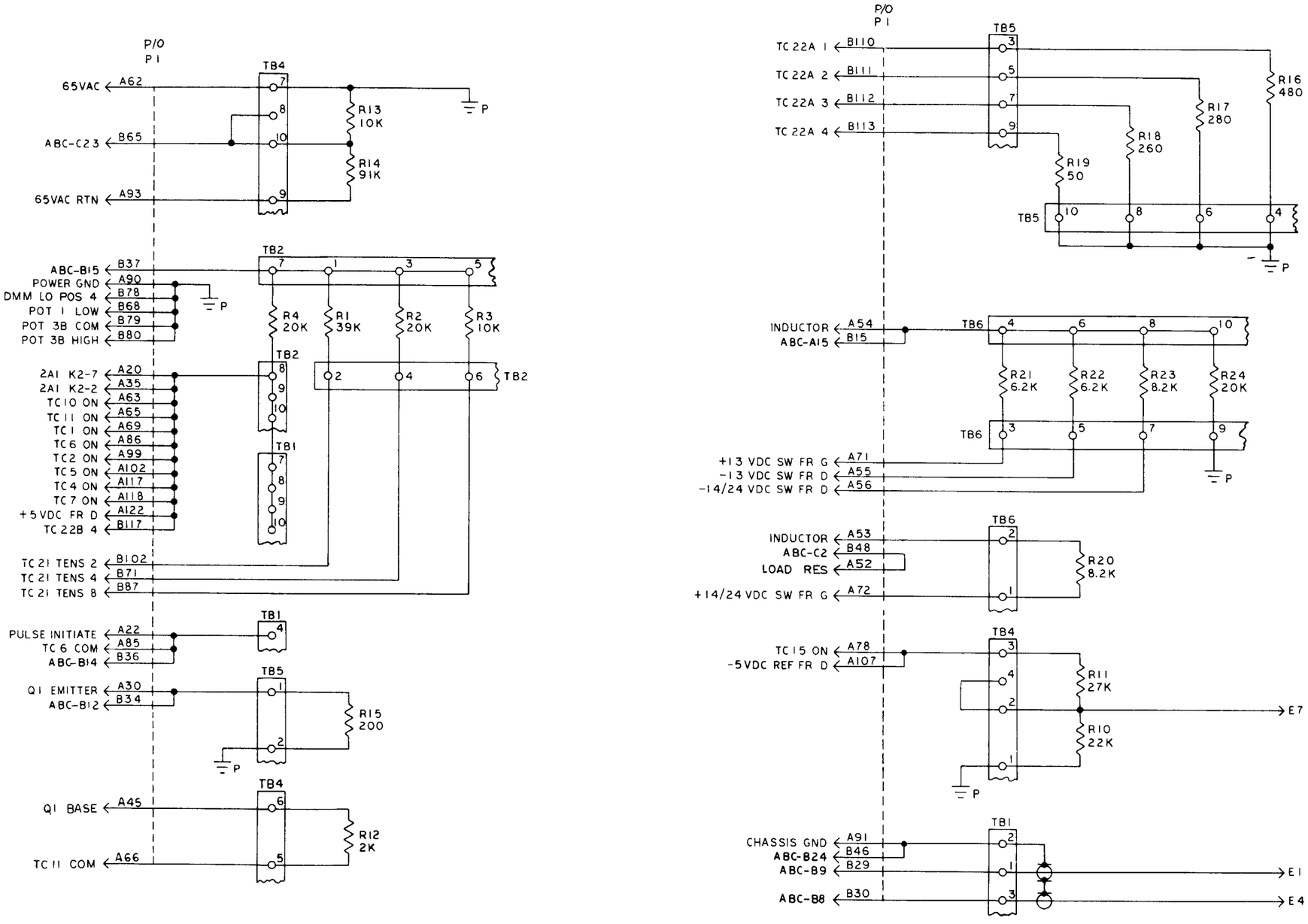


Figure 5-14. DMS-G test adapter A8 (10275275)-schematic diagram (sheet 2 of 2)

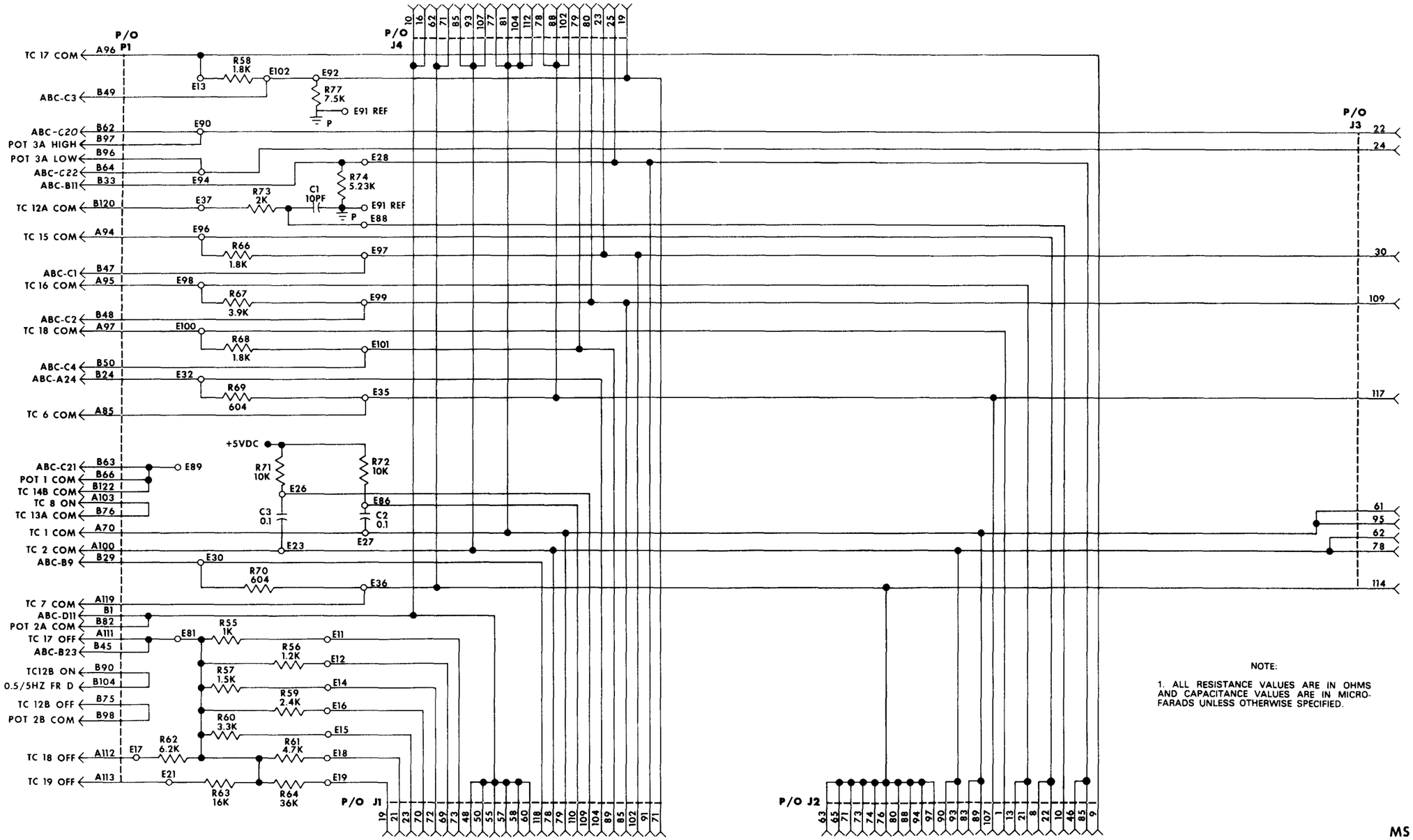
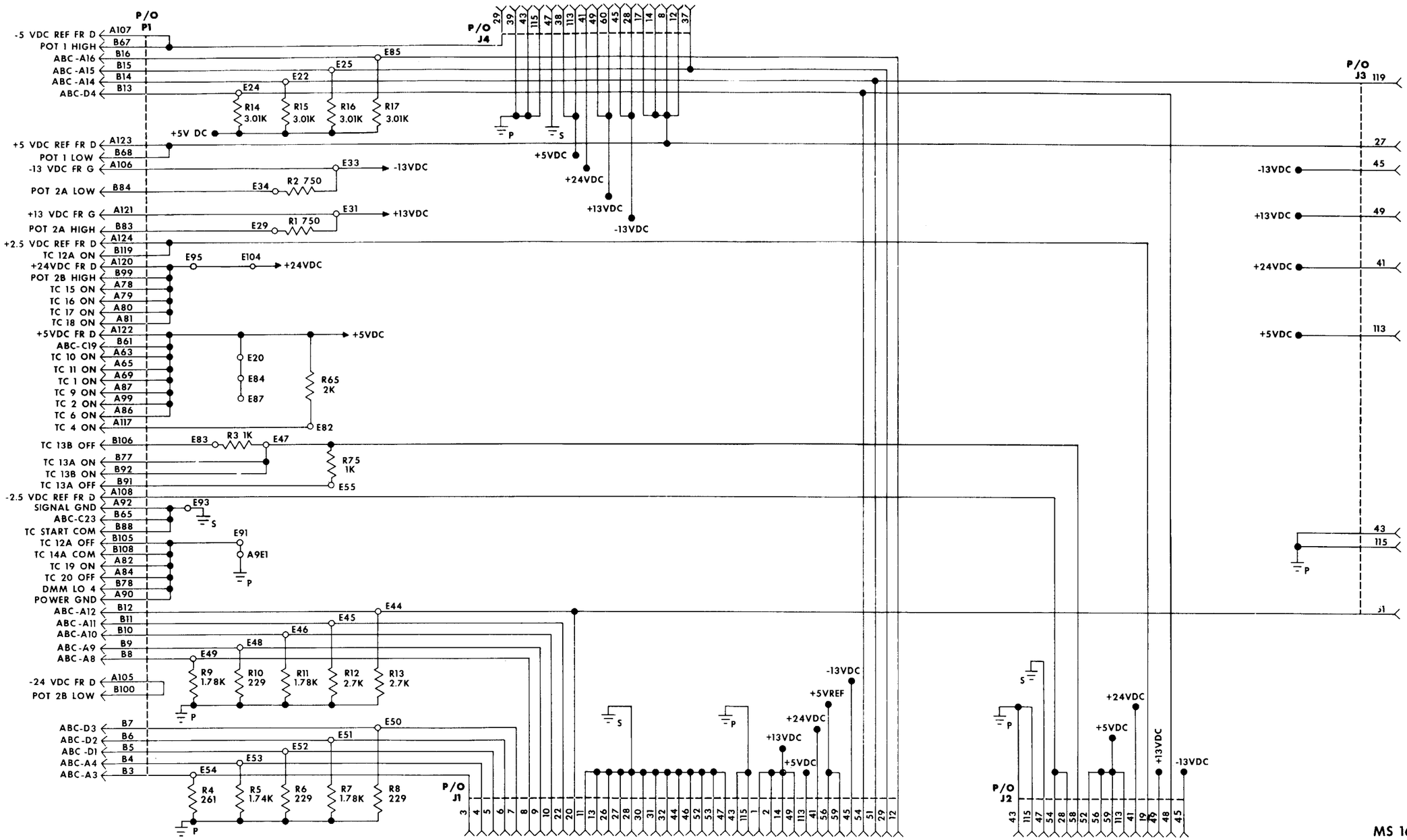


Figure 5-15. DMS-G test adapter A9 schematic diagram (sheet 1 of 4)



MS 161314

Figure 5-15. DMS-G test adapter A9 (10275276)-schematic diagram (sheet 2 of 4)

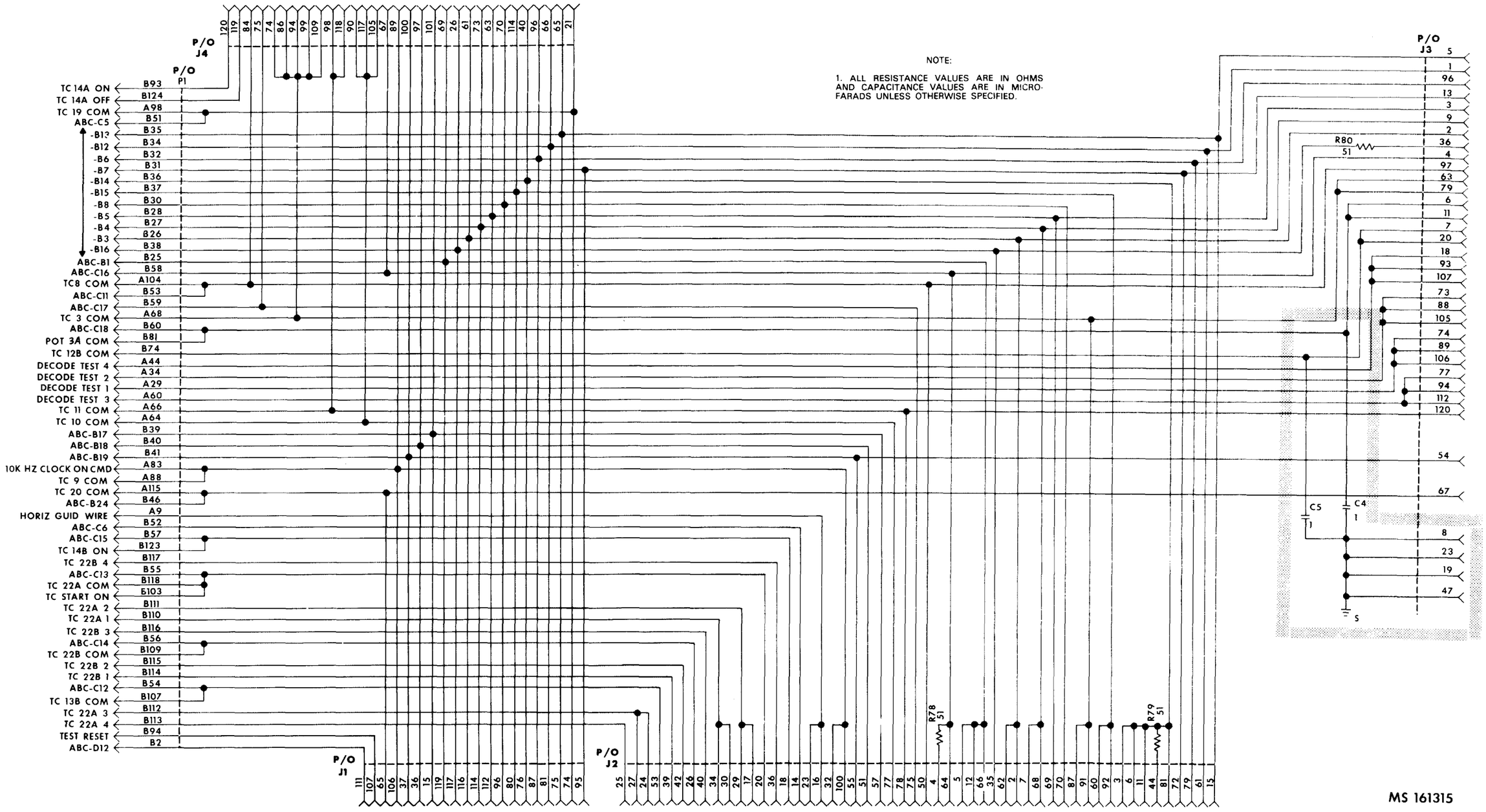


Figure 5-15. DMS-G test adapter A9 schematic diagram (sheet 3 of 4)

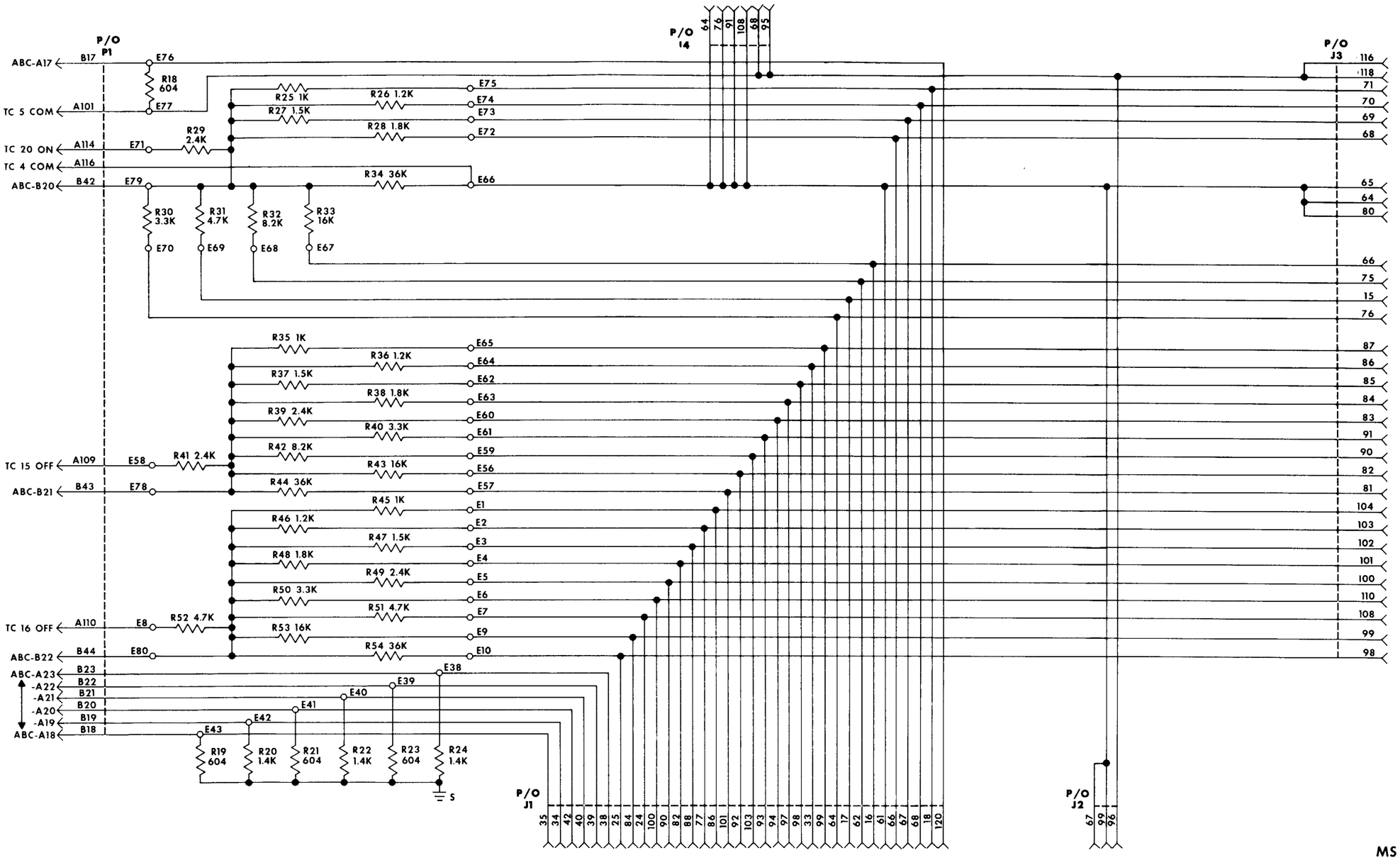
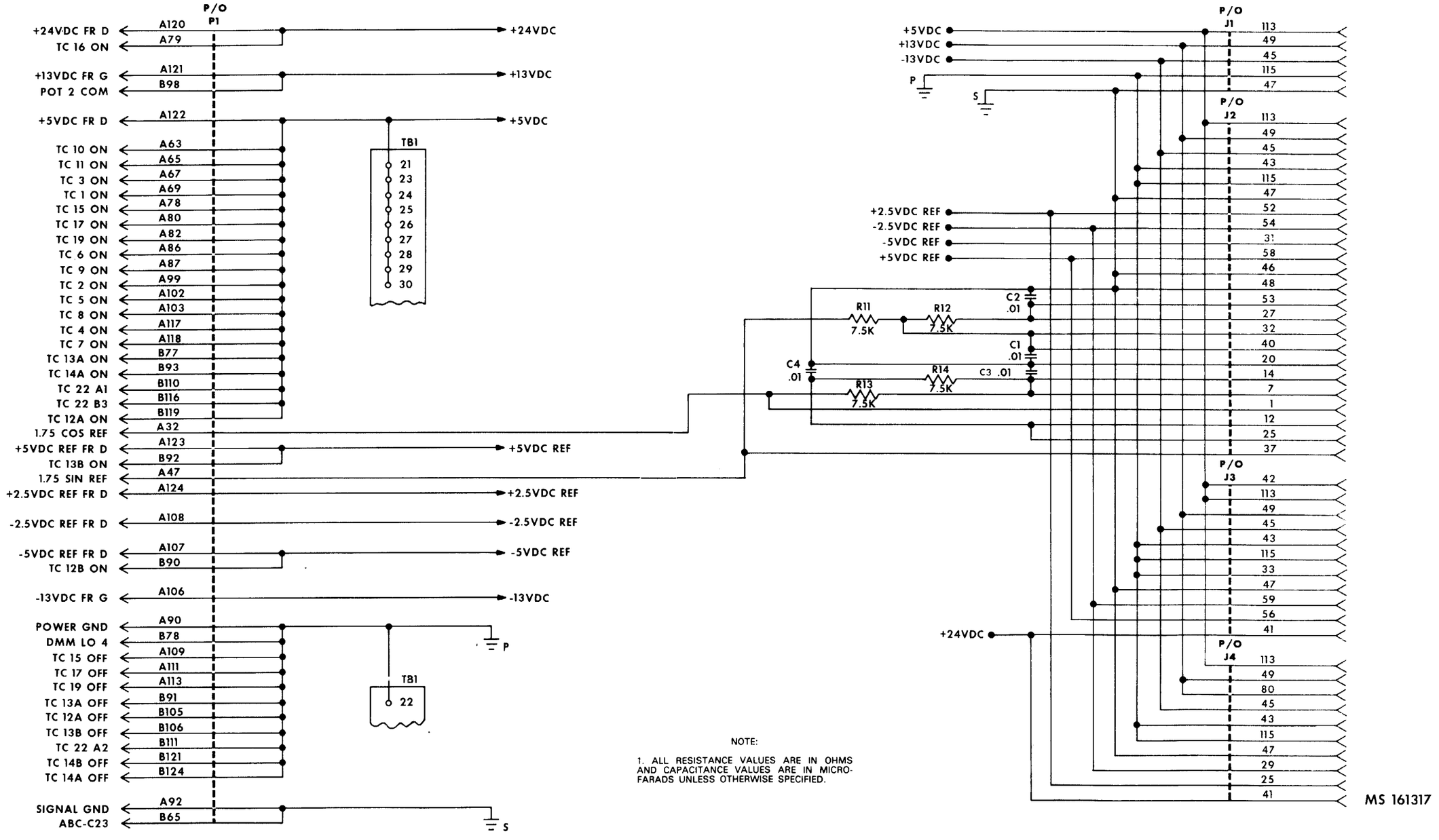


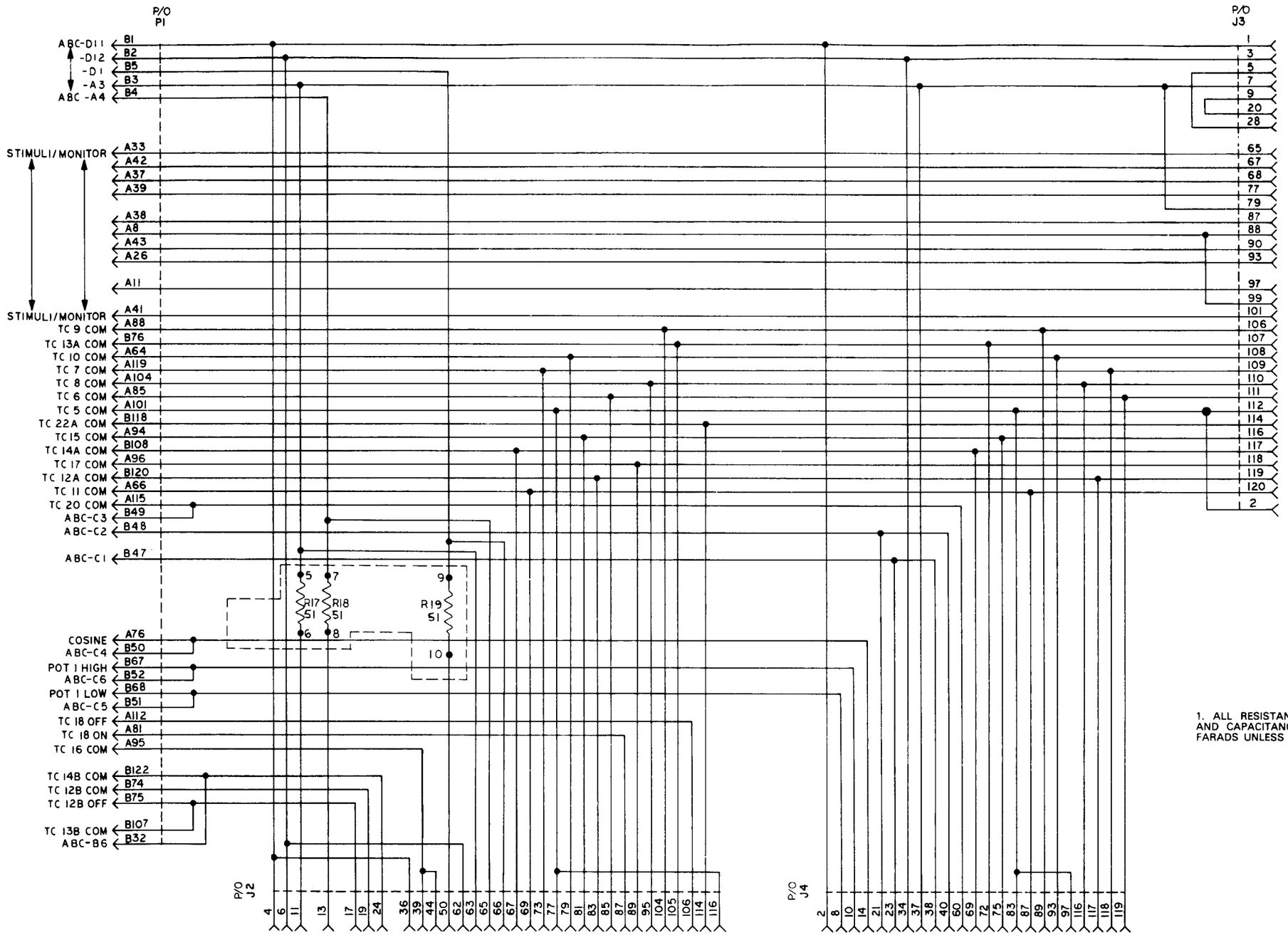
Figure 5-15. DMS-G test adapter A9 - schematic diagram (sheet 4 of 4)



NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

Figure 5-16. DMS-G test adapter A10 schematic diagram (sheet 1 of 3)



NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

MS 161318

Figure 5-16. DMS-G test adapter A10 schematic diagram (sheet 2 of 3)

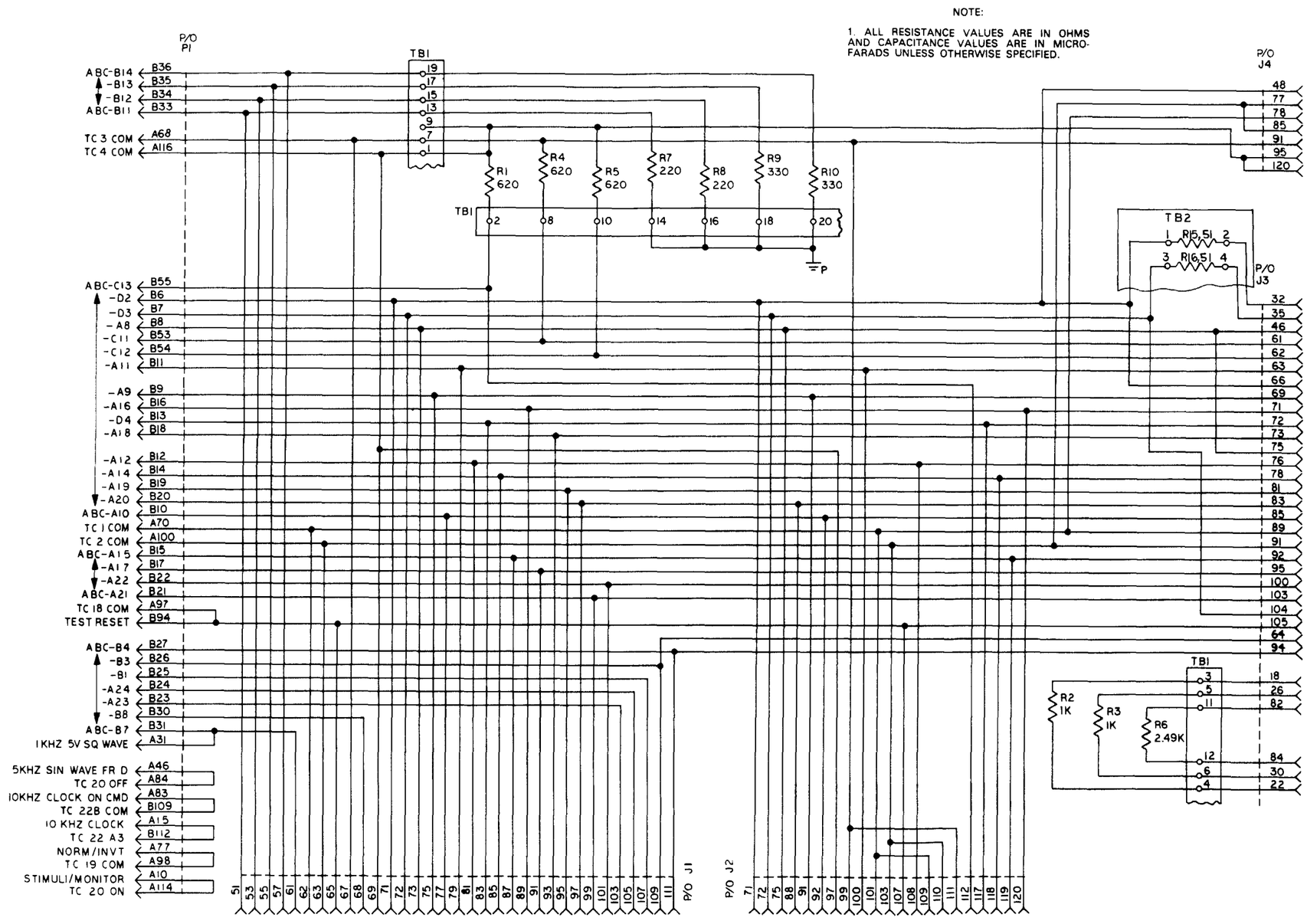


Figure 5-16. DMS-G test adapter A10 schematic diagram (sheet 3 of 3)

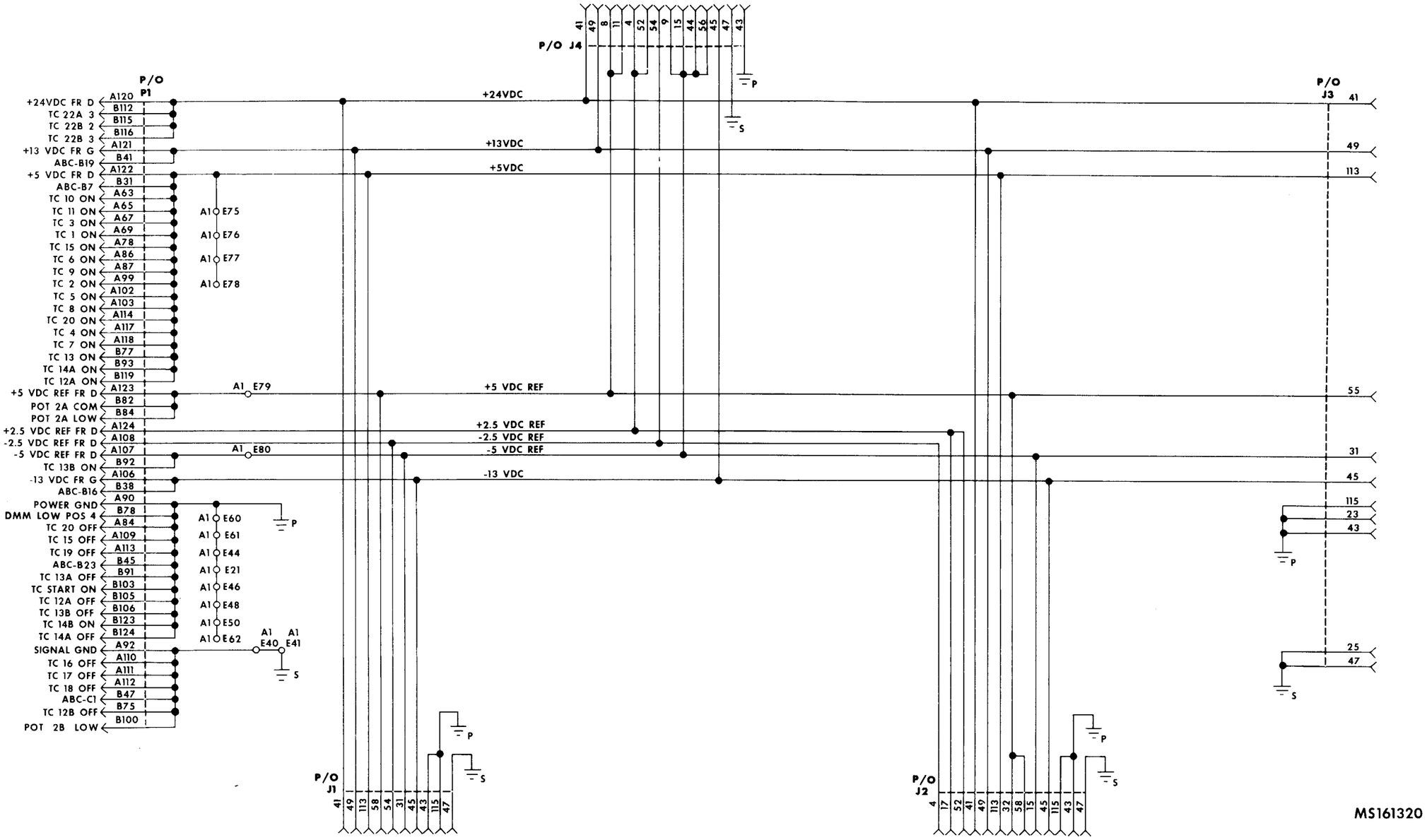
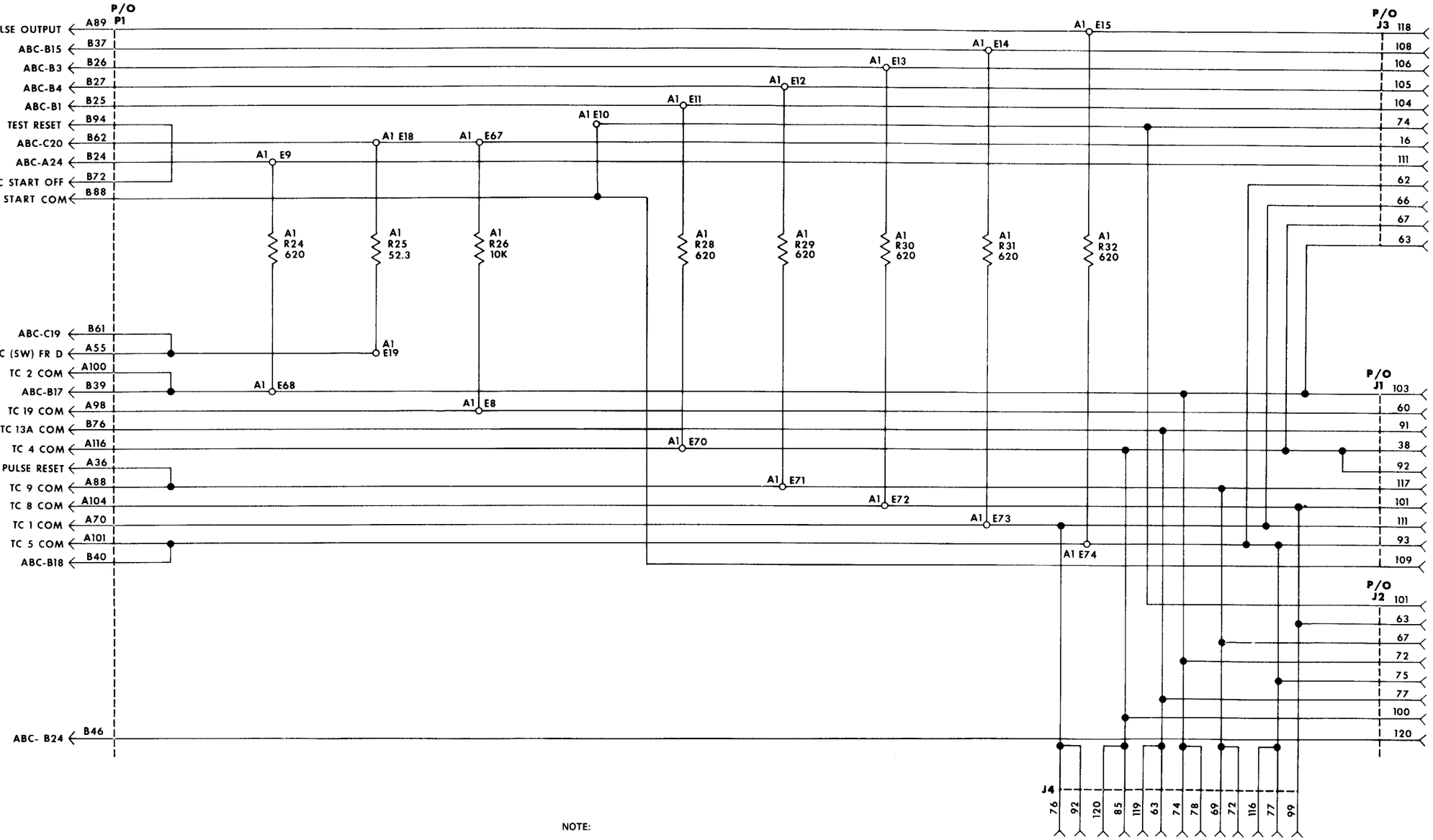


Figure 5-17. DMS-G test adapter All schematic diagram (sheet 1 of 4)

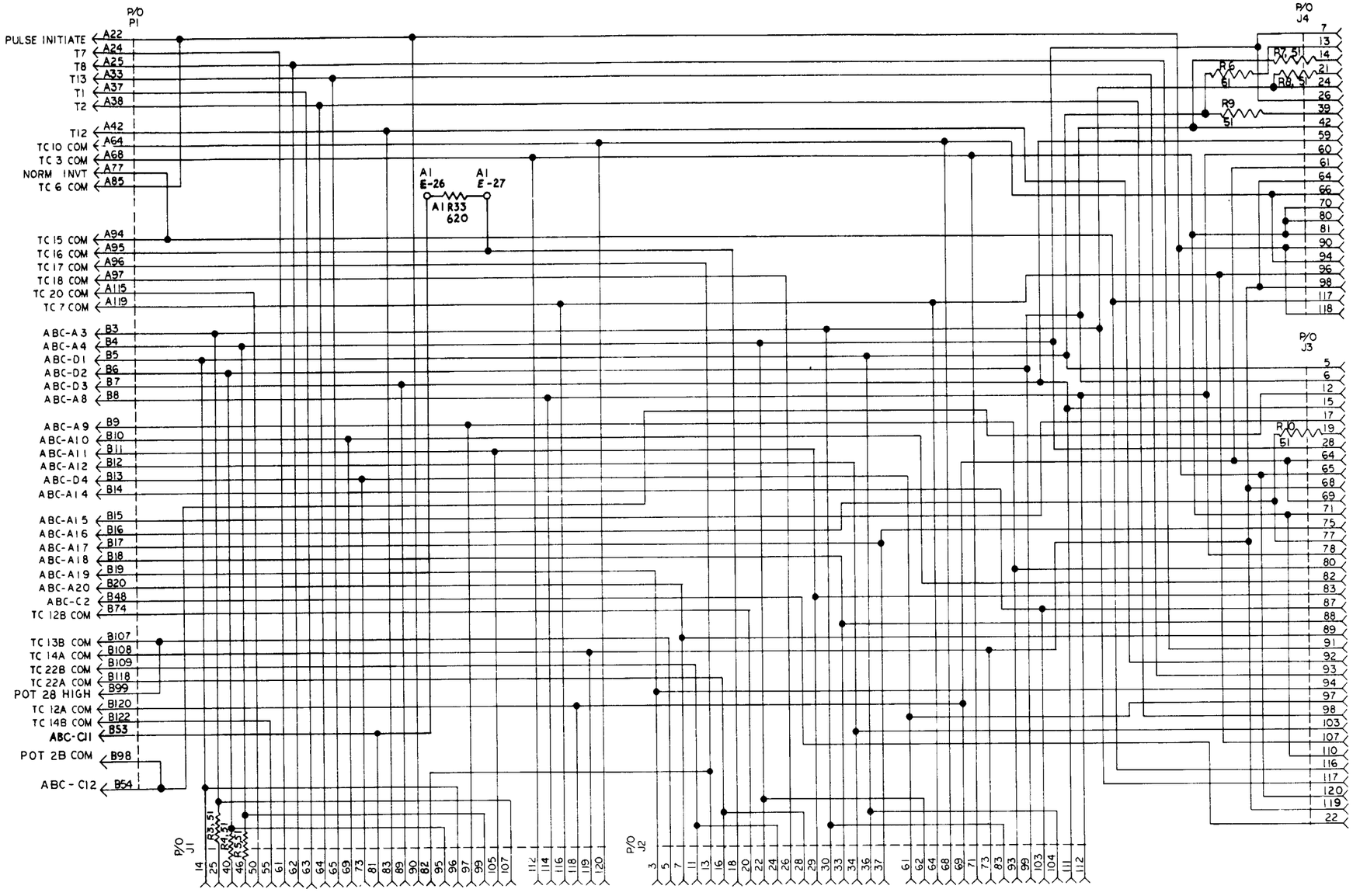


NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICRO-FARADS UNLESS OTHERWISE SPECIFIED.

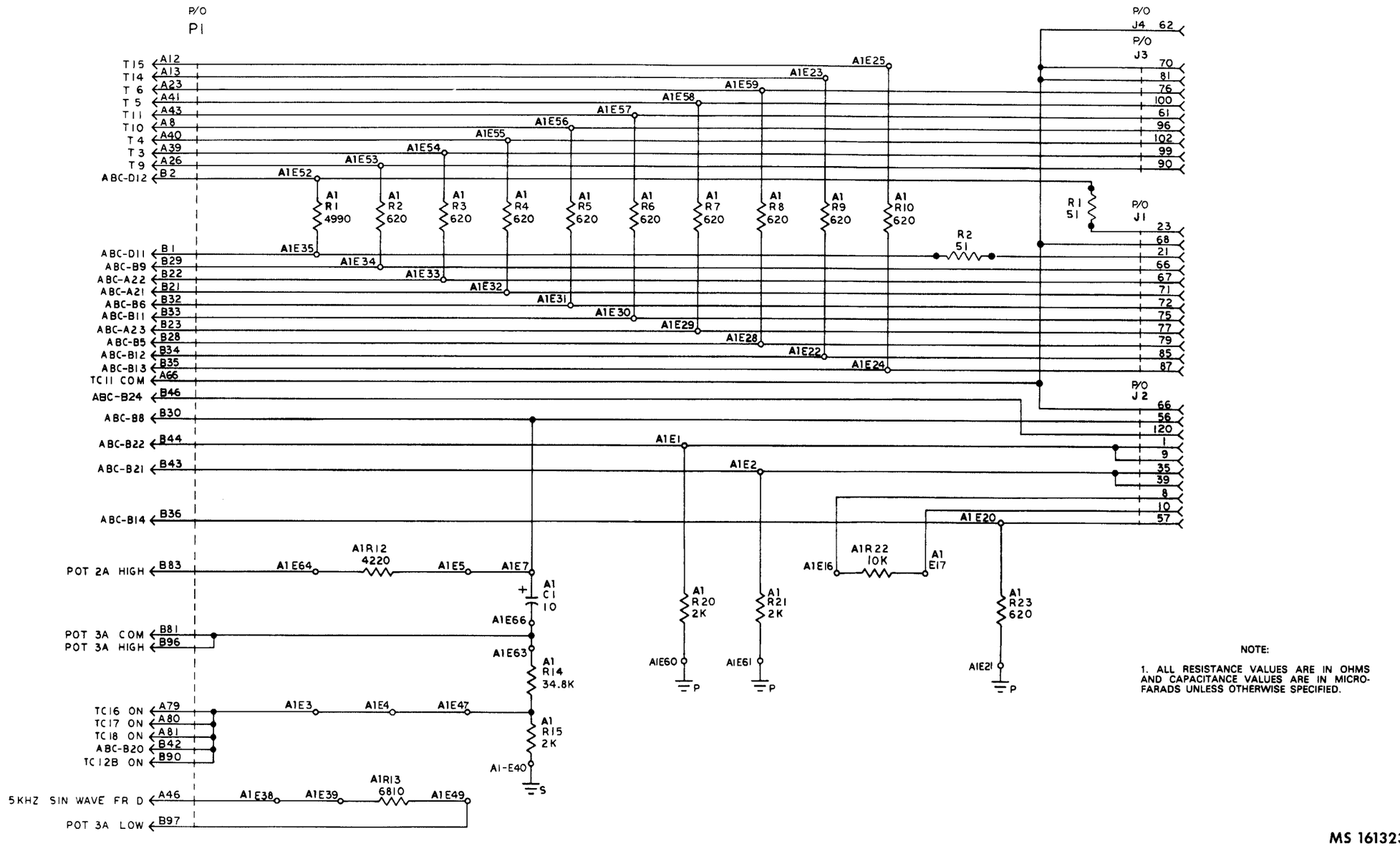
MS161321

Figure 5-17. DMS-G test adapter All schematic diagram (sheet 2 of 4)



MS 161322

Figure 5-17. DMS-G test adapter A11-schematic diagram (sheet 3 of 4)



NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

MS 161323

Figure 5-17. DMS-G test adapter A11-schematic diagram (sheet 4 of 4)

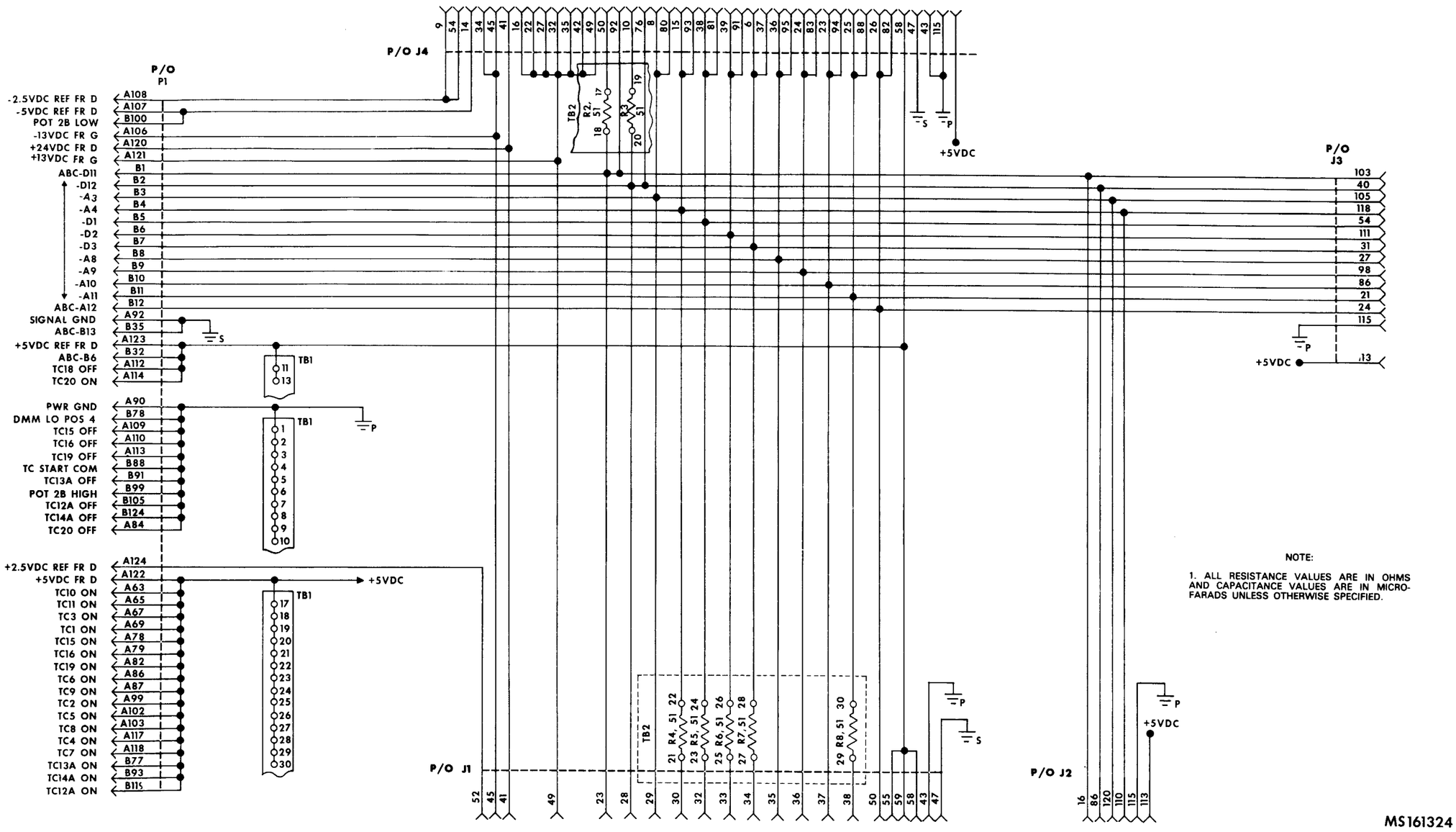
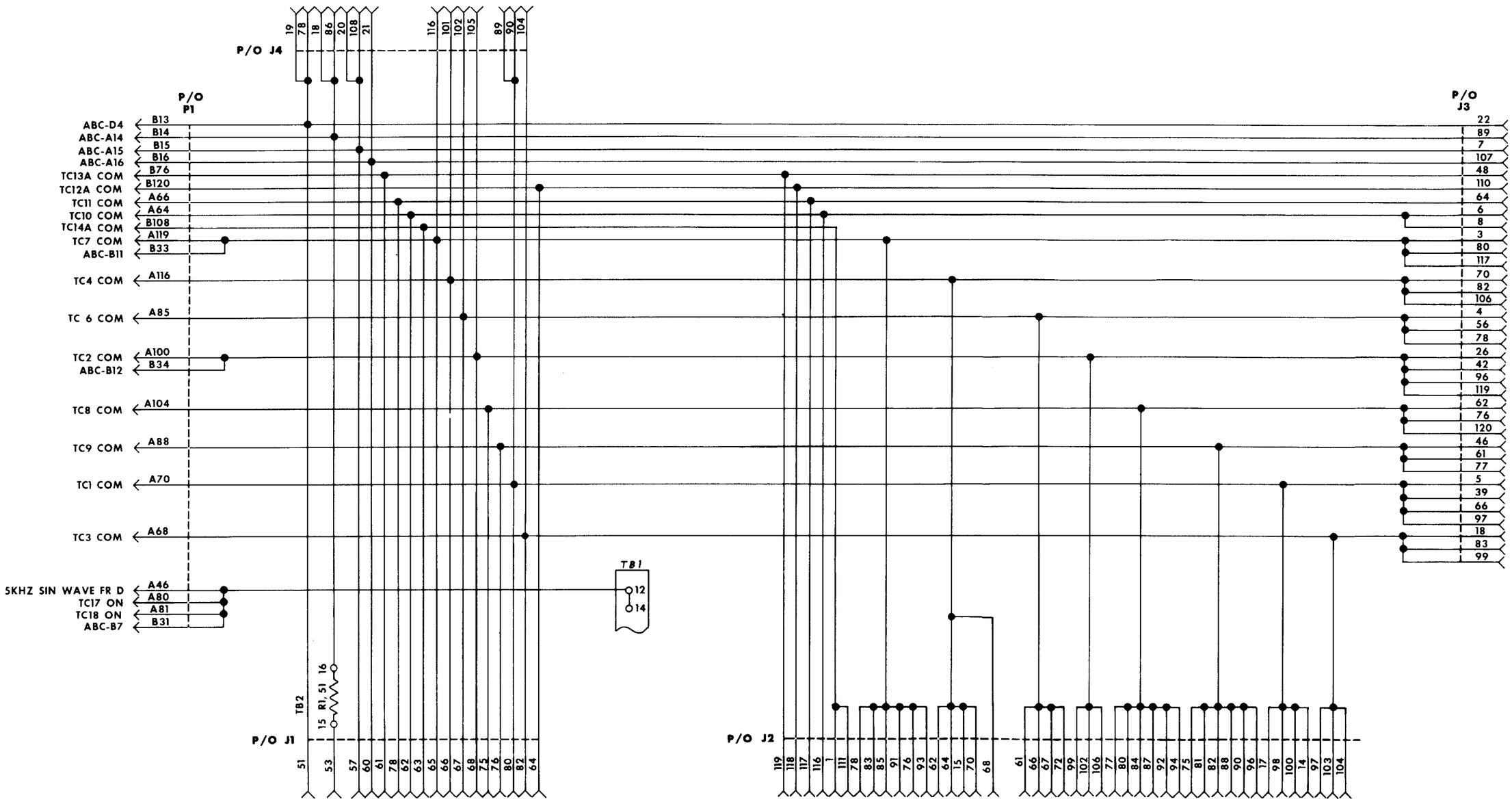


Figure 5-18. DMS-G test adapter A12-schematic diagram (sheet 1 of 3)



MS 161325

Figure 5-18. DMS-G test adapter A12 schematic diagram (sheet 2 of 3)

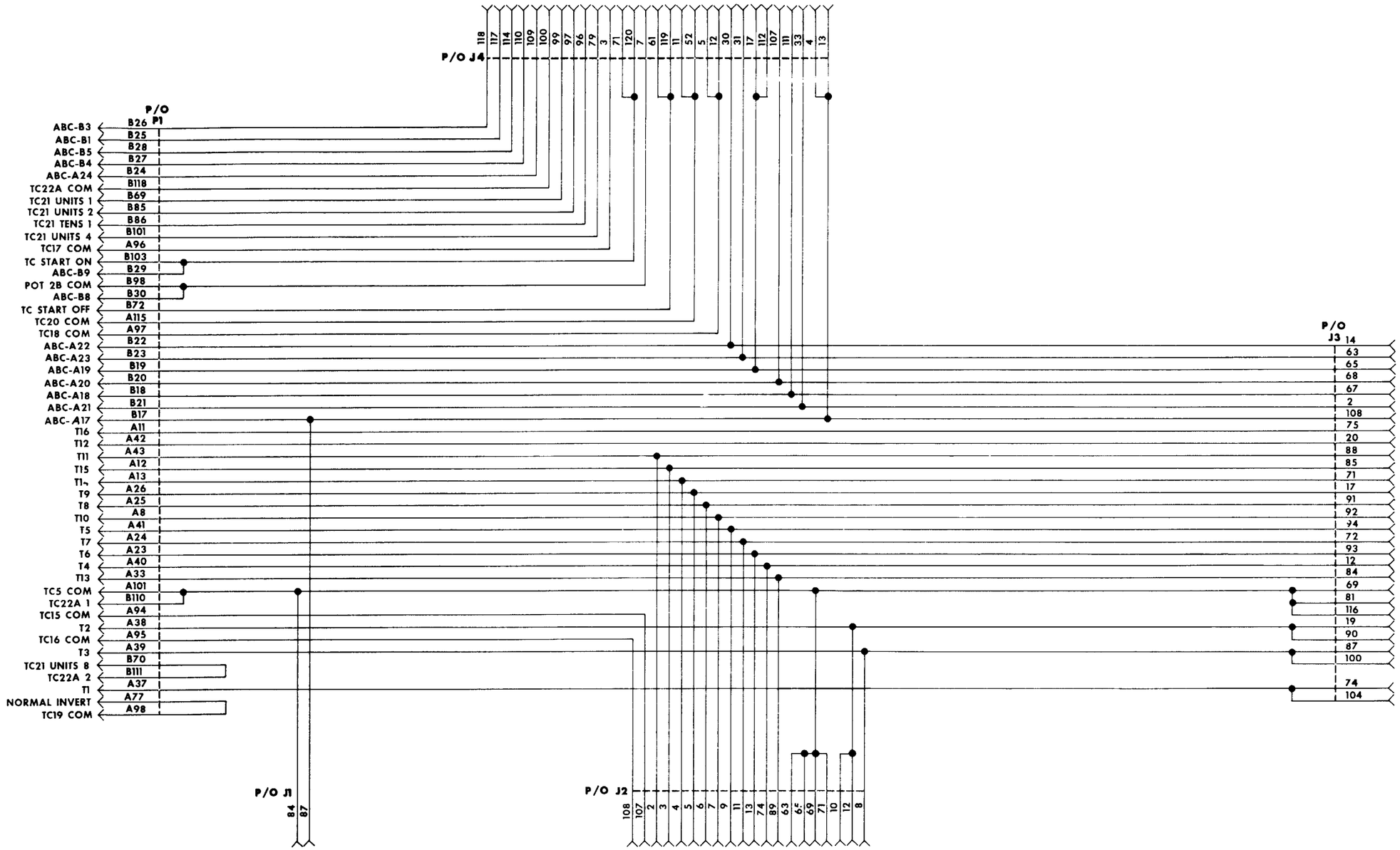
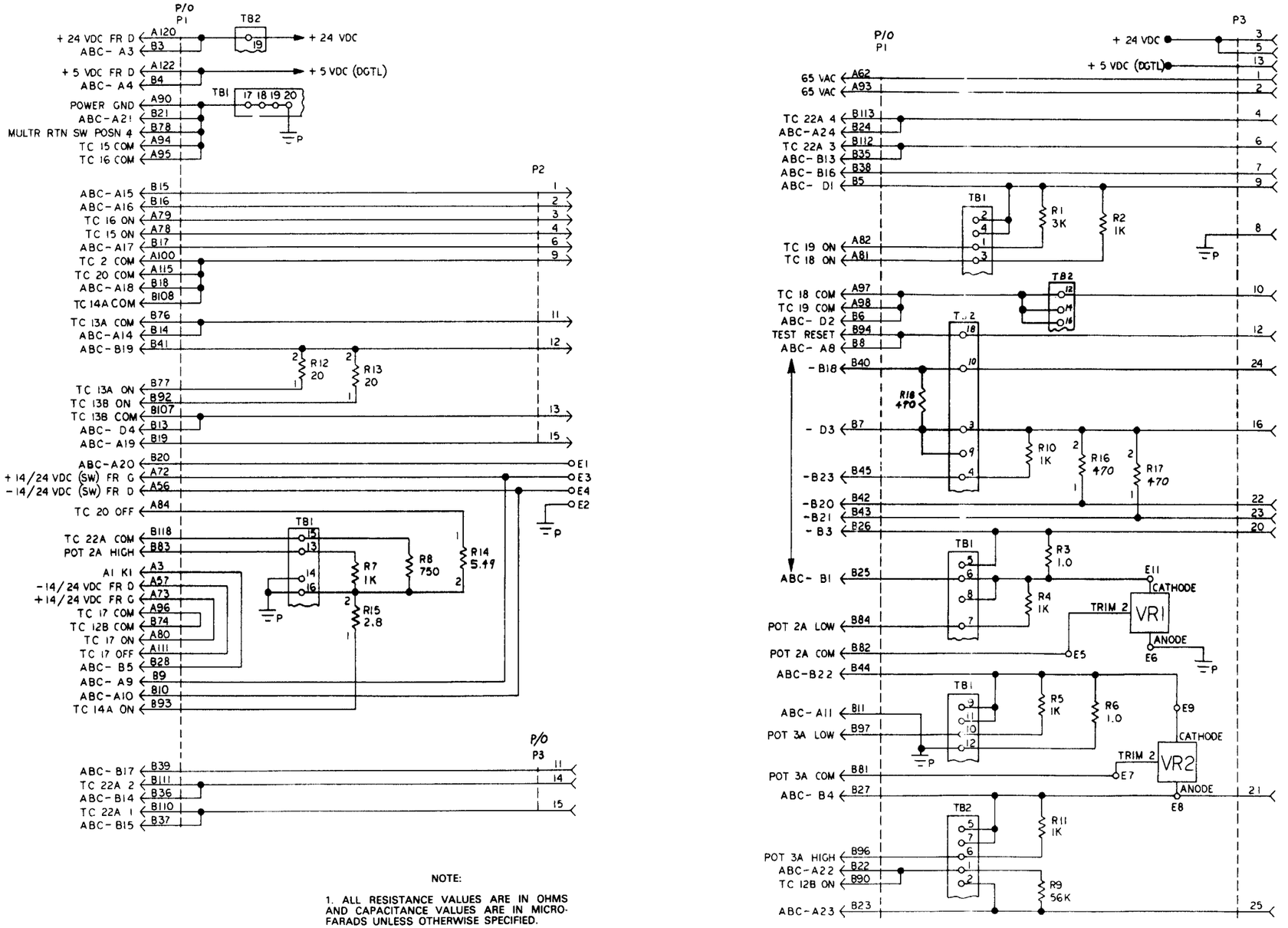


Figure 5-18. DMS-G test adapter A12-schematic diagram (sheet 3 of 3)

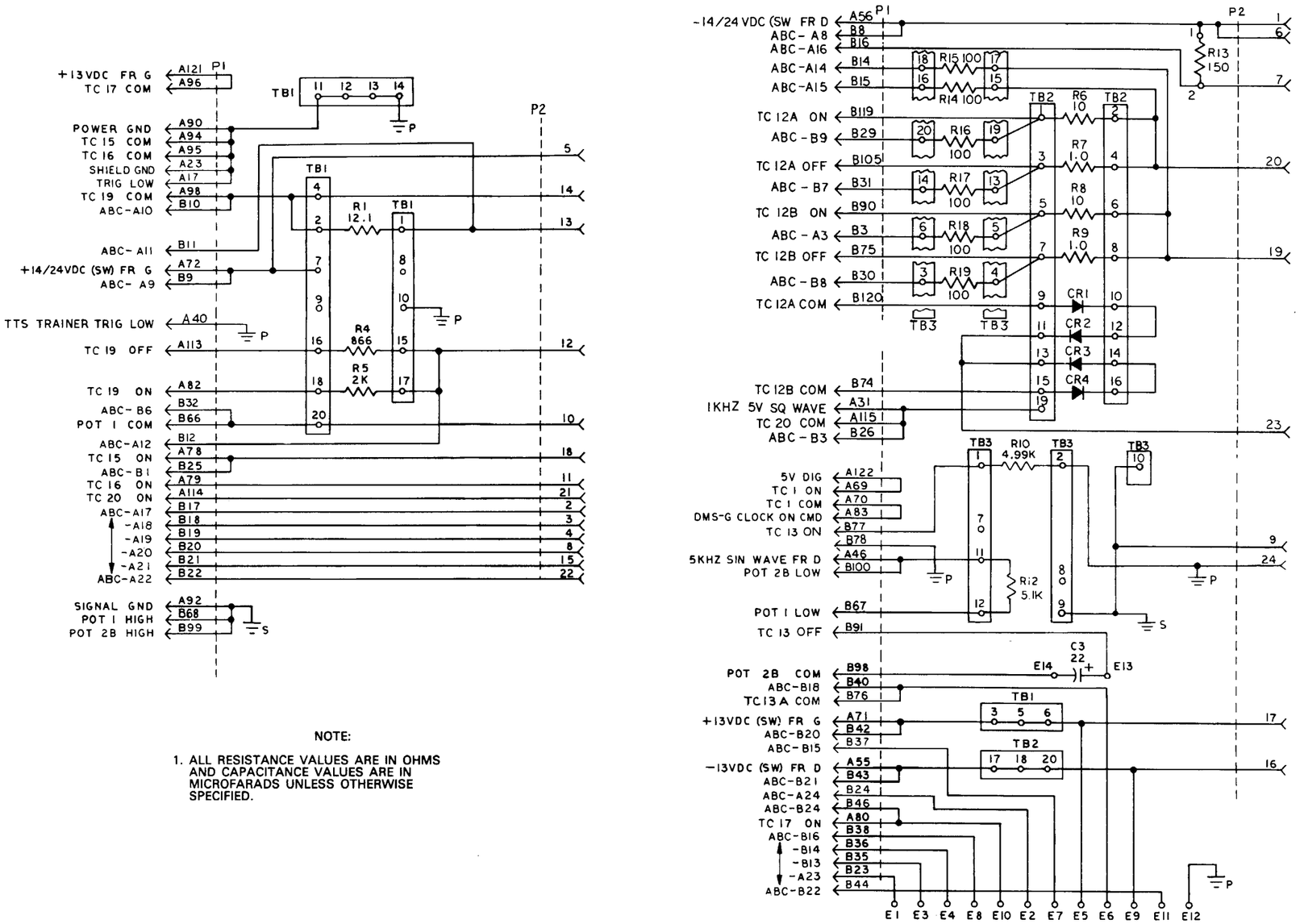


NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

MS 161327

Figure 5-19. DMS-G test adapter A13-schematic diagram



NOTE:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

MS 161328

Figure 5-20. DMS-G test adapter A14 schematic diagram

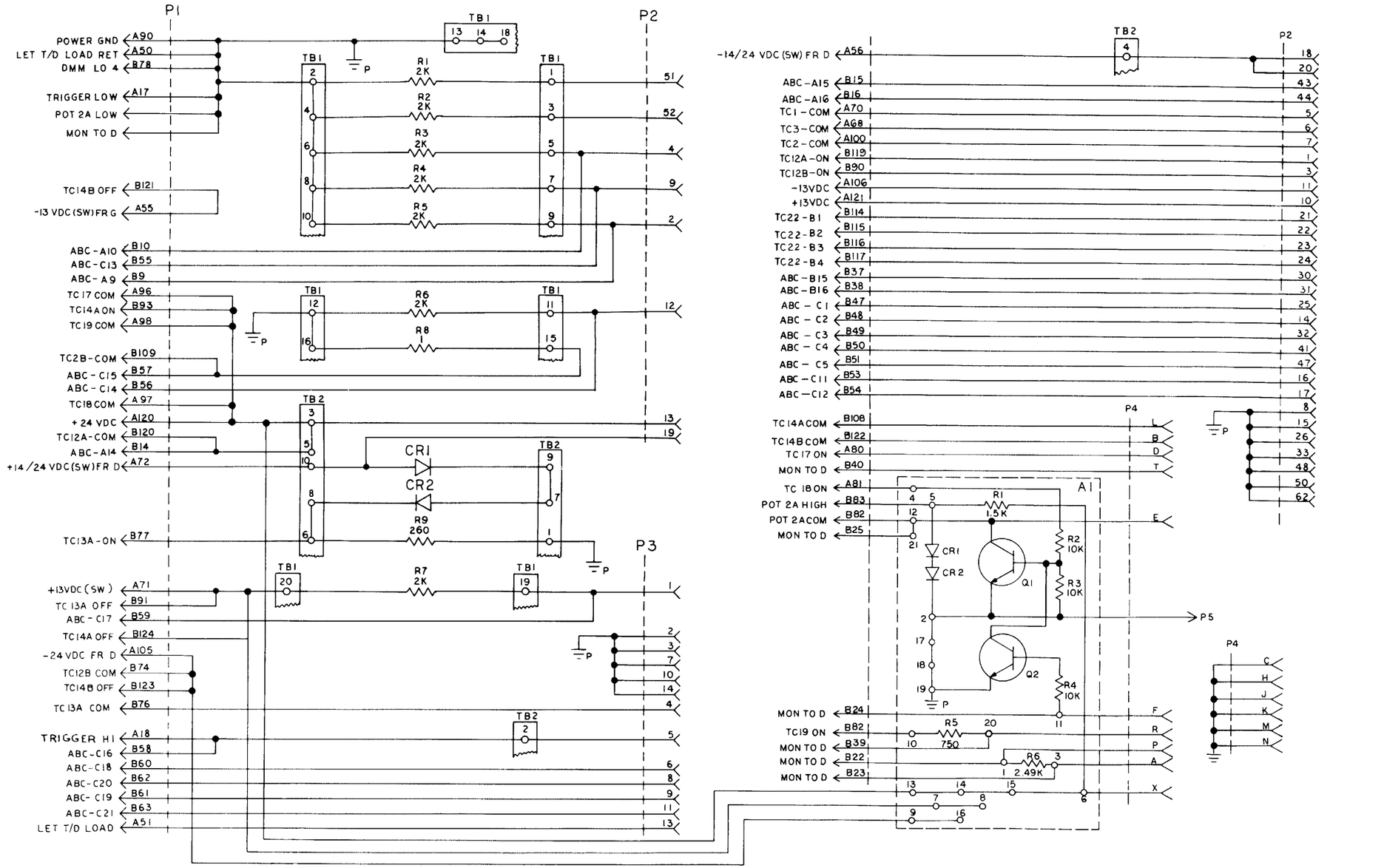


Figure 5-21. Test adapter A15 (10275956) schematic diagram

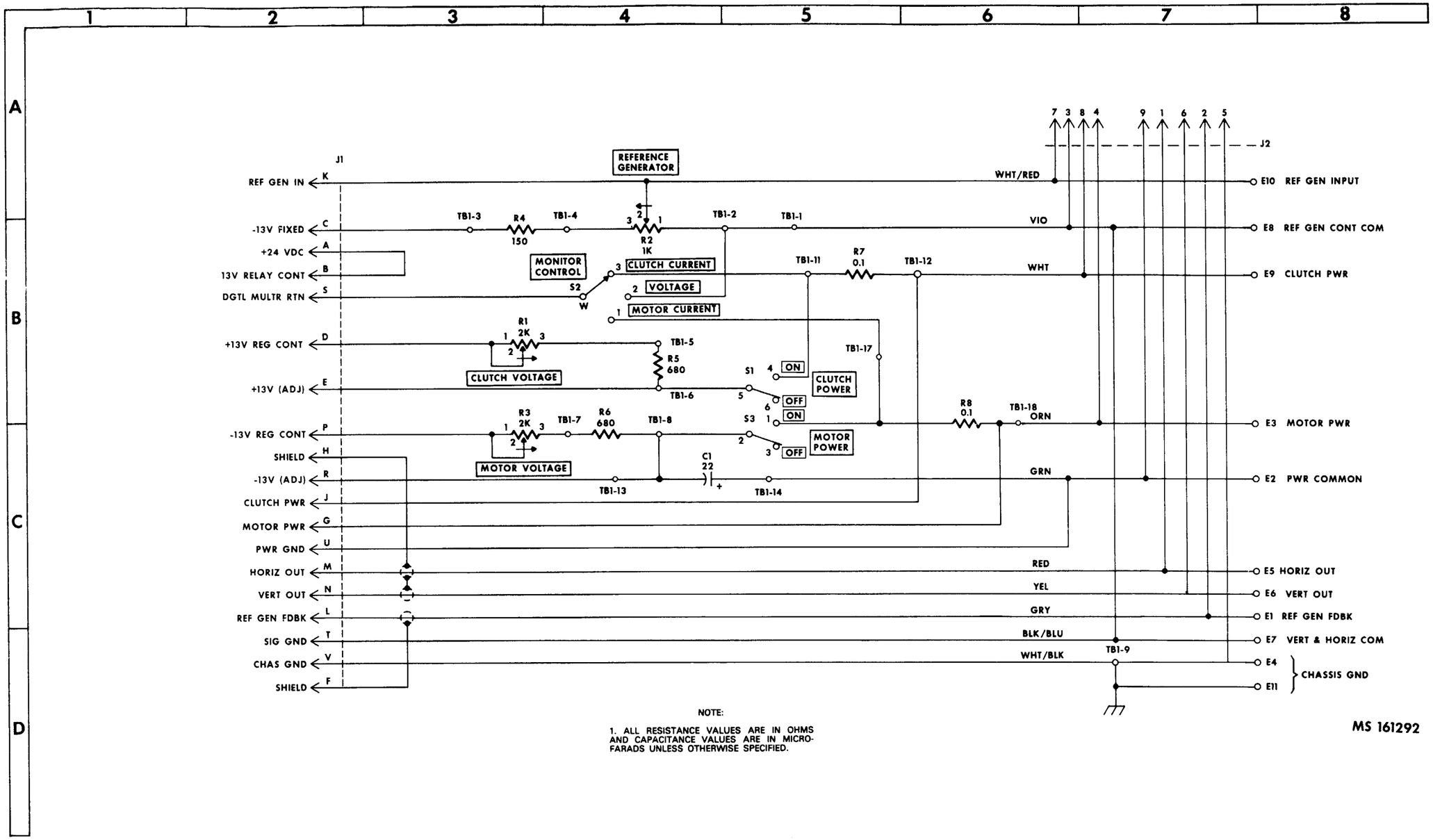


Figure 5-22. Nutator test adapter schematic diagram

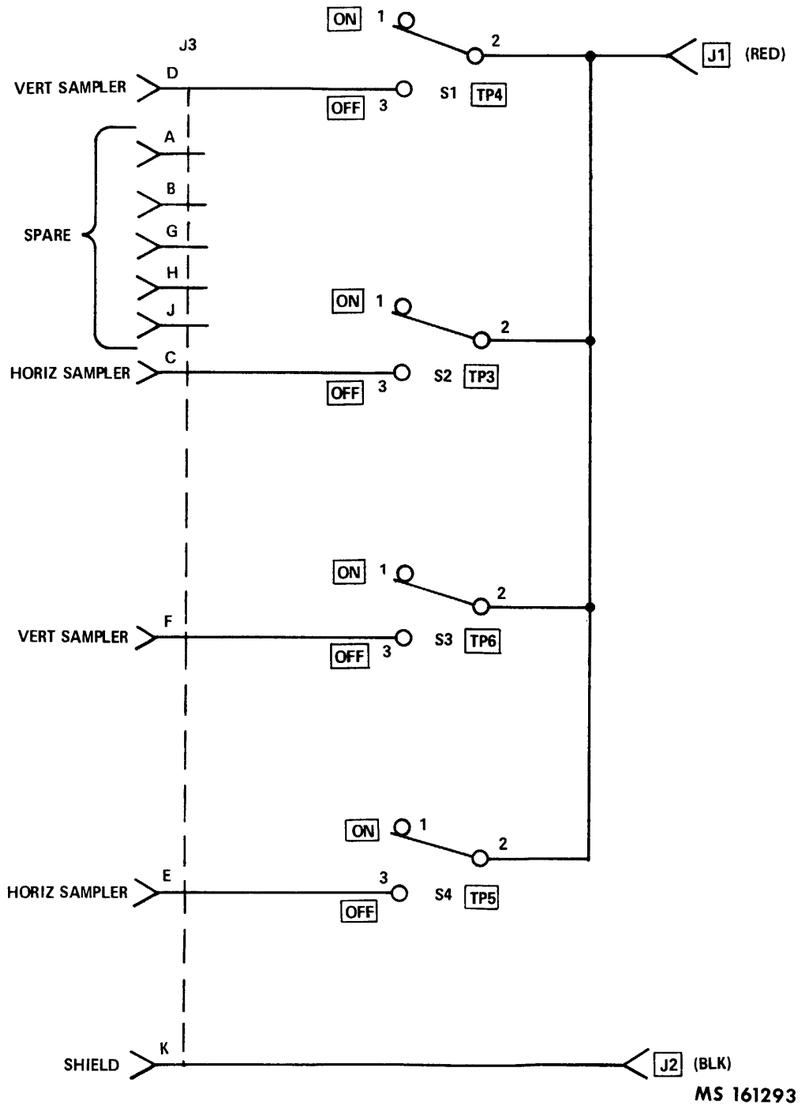


Figure 5-22. Test phase control adapter -schematic diagram

CHAPTER 6

QQ - SCHEMATIC DIAGRAMS

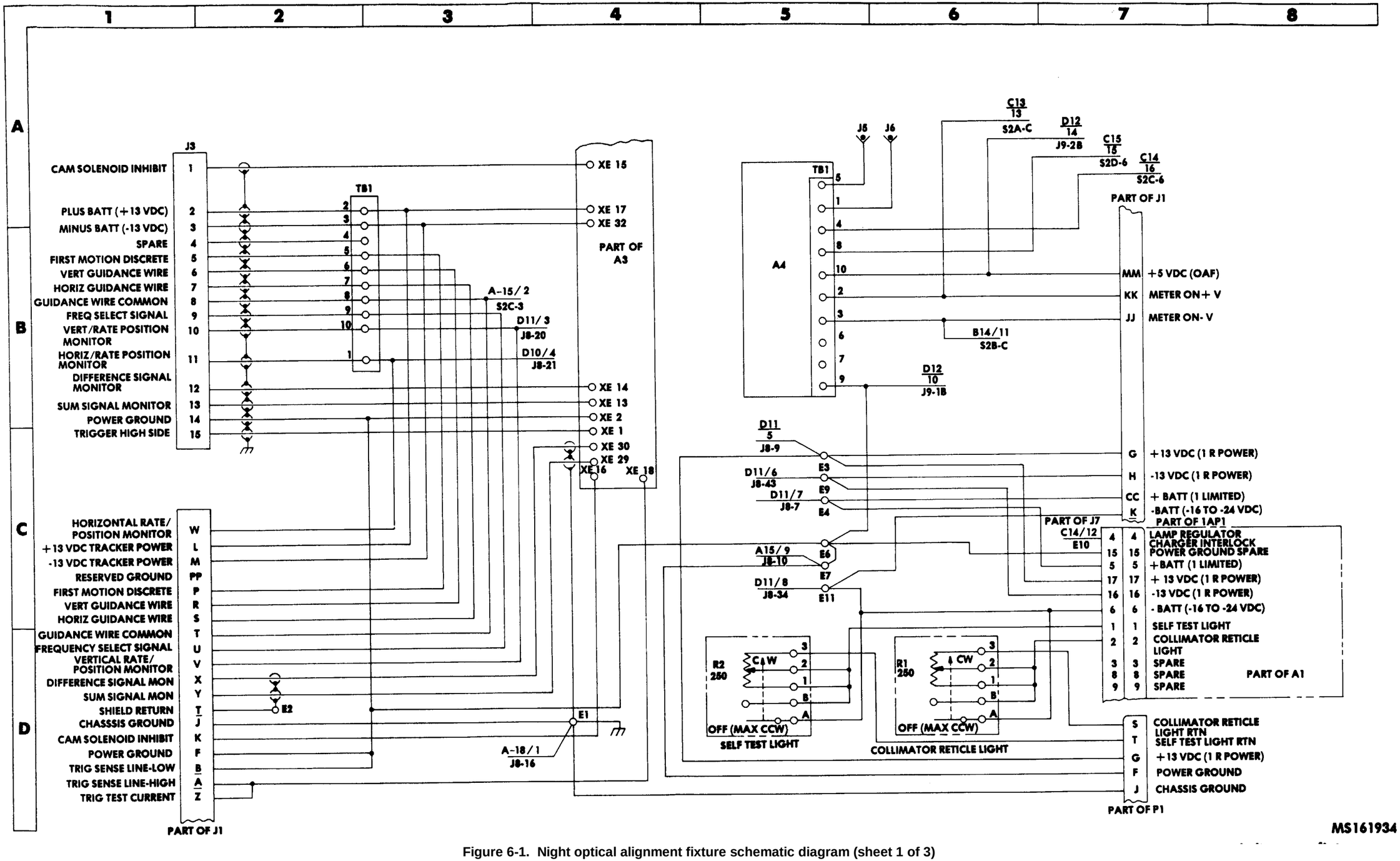


Figure 6-1. Night optical alignment fixture schematic diagram (sheet 1 of 3)

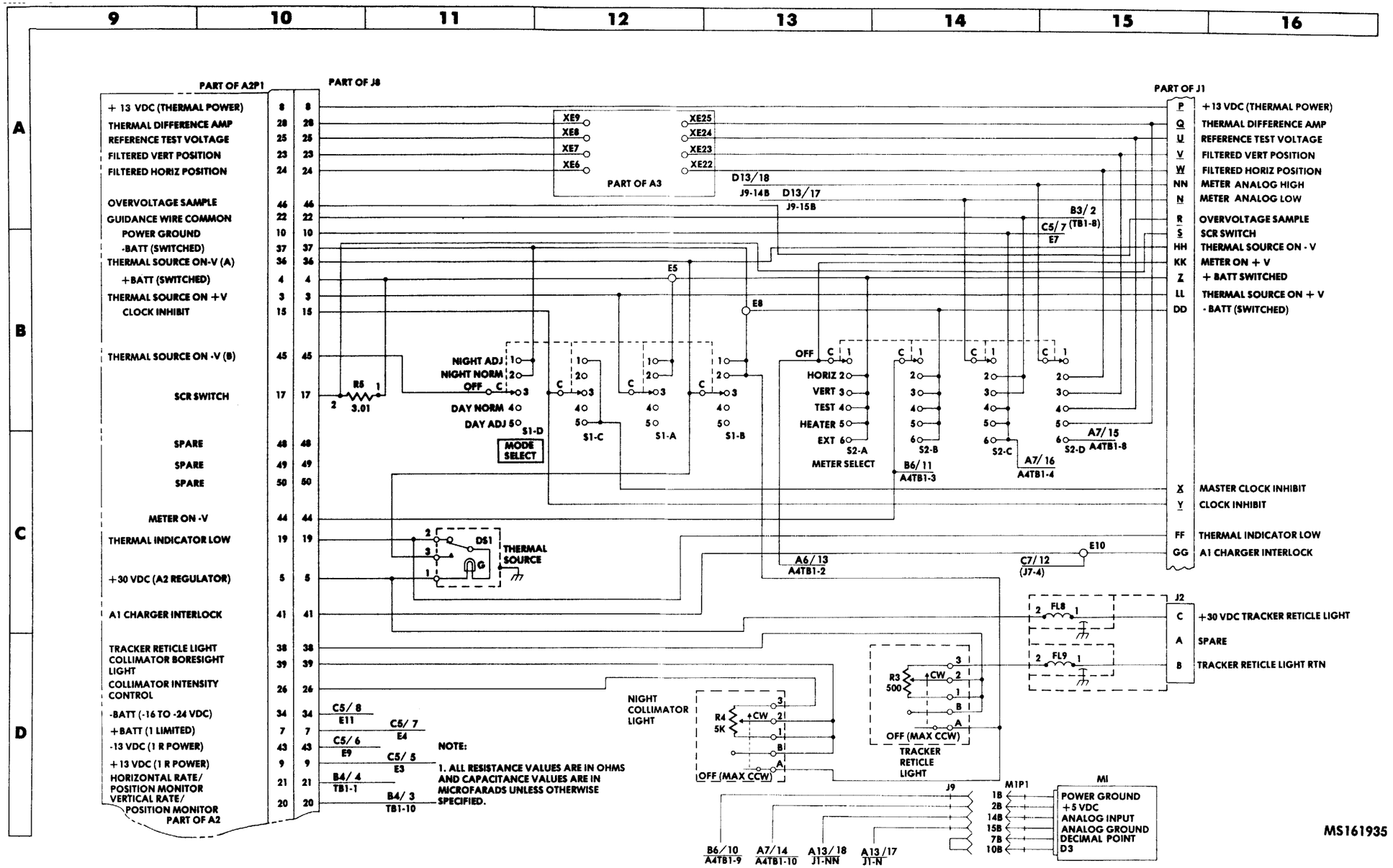


Figure 6-1. Night optical alignment fixture schematic diagram (sheet 2 of 3)

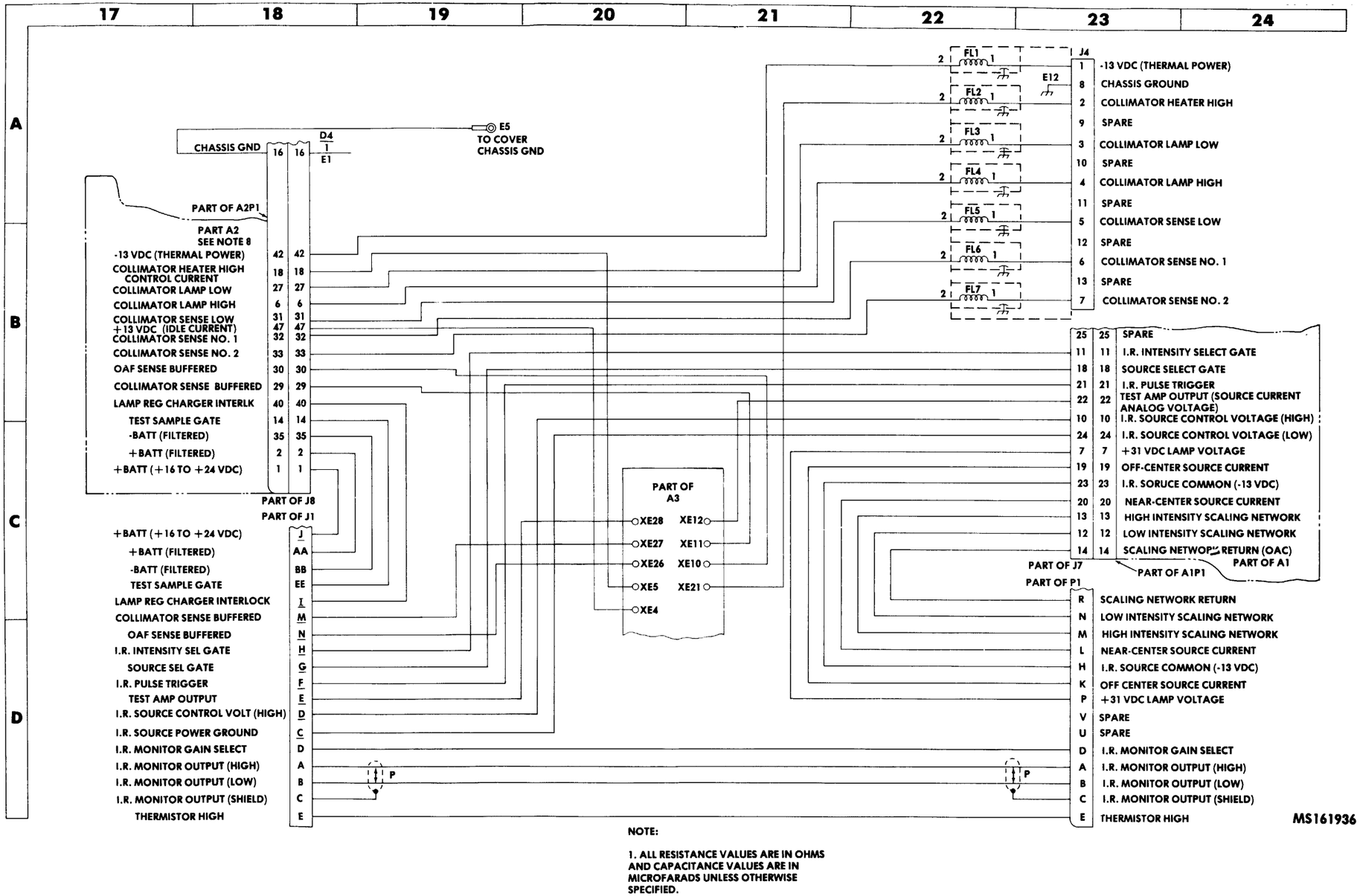
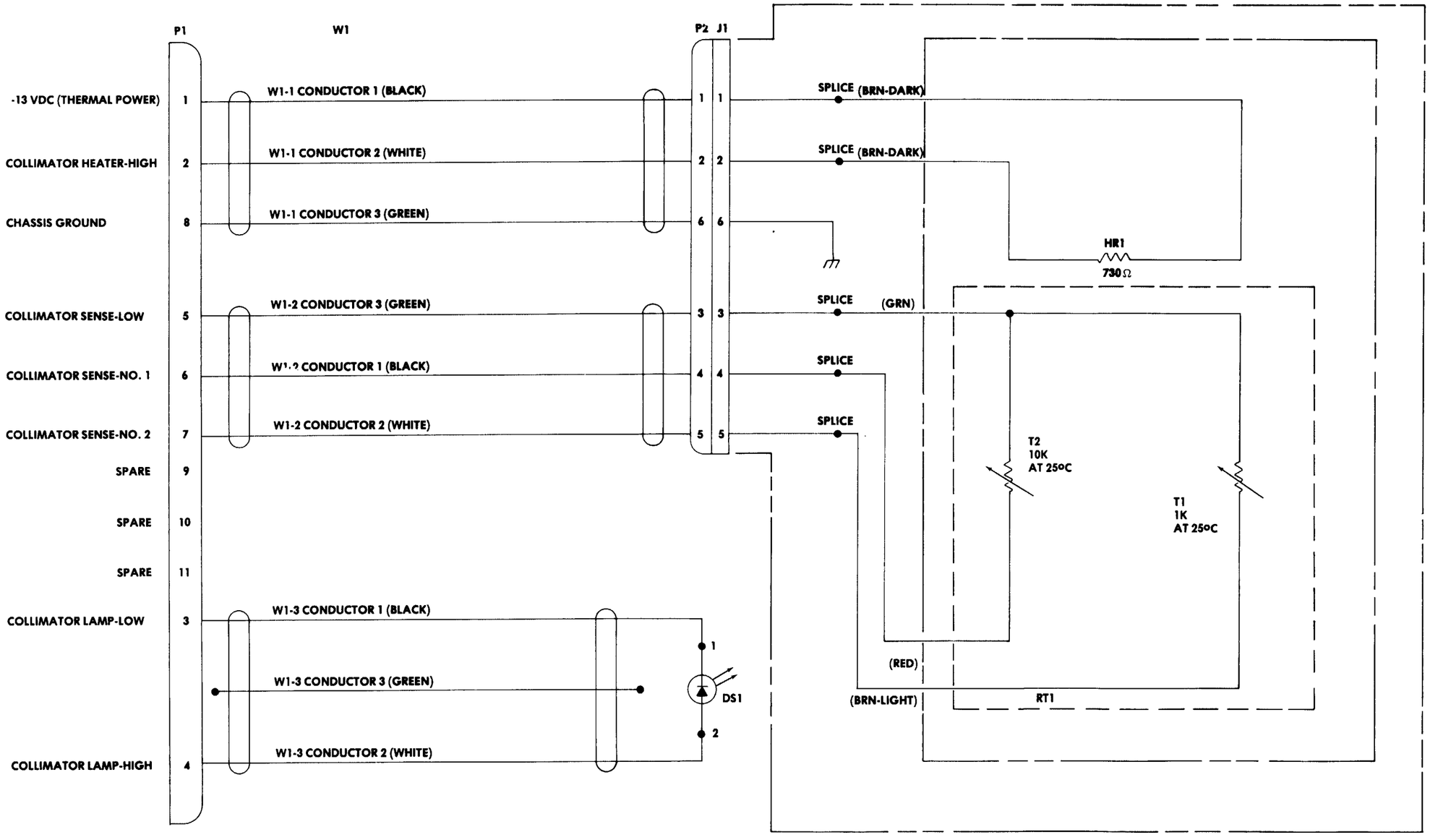


Figure 6-1. Night optical alignment fixture schematic diagram (sheet 3 of 3)



MS161937

Figure 6-2. Thermal collimator schematic diagram

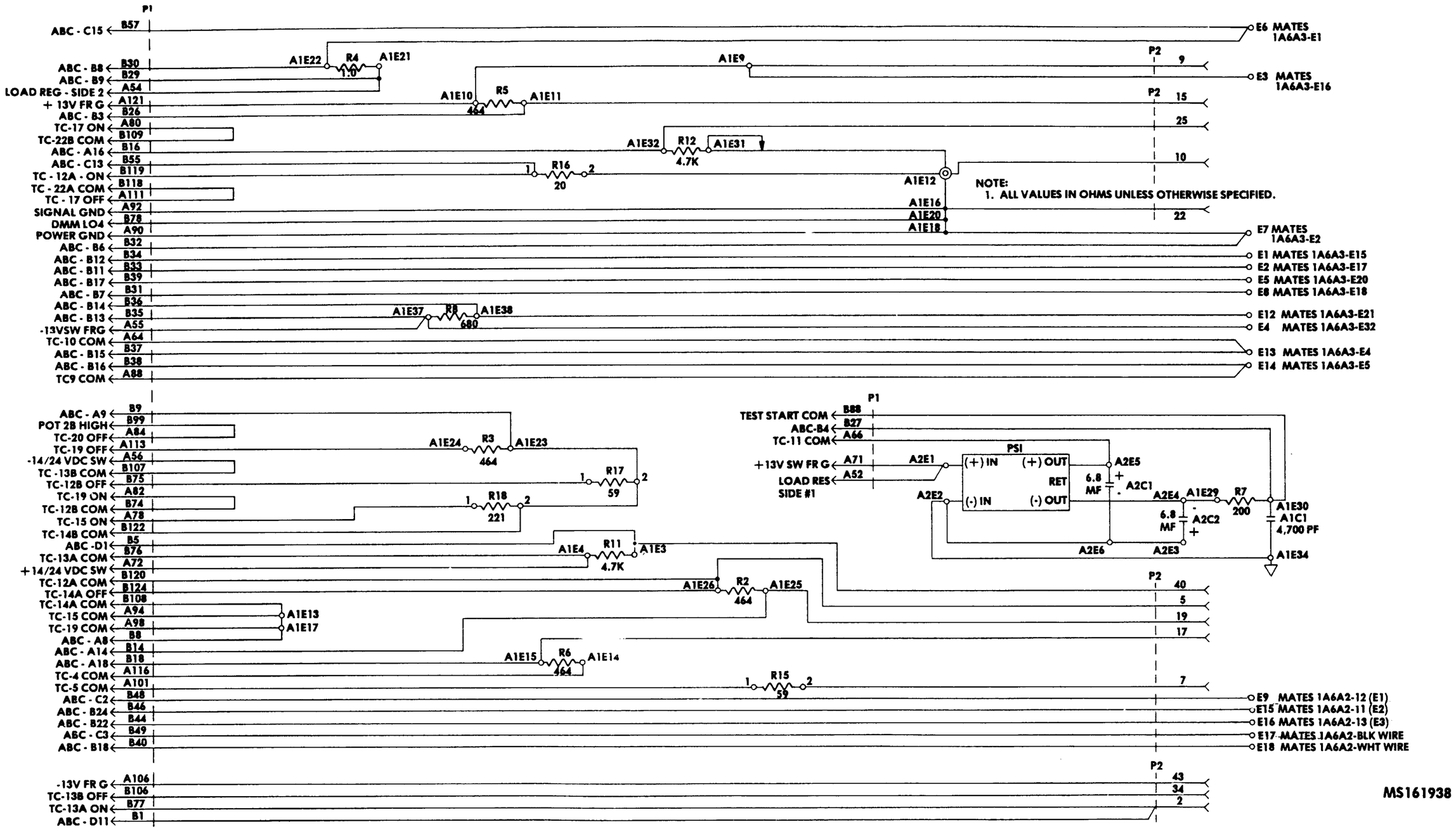
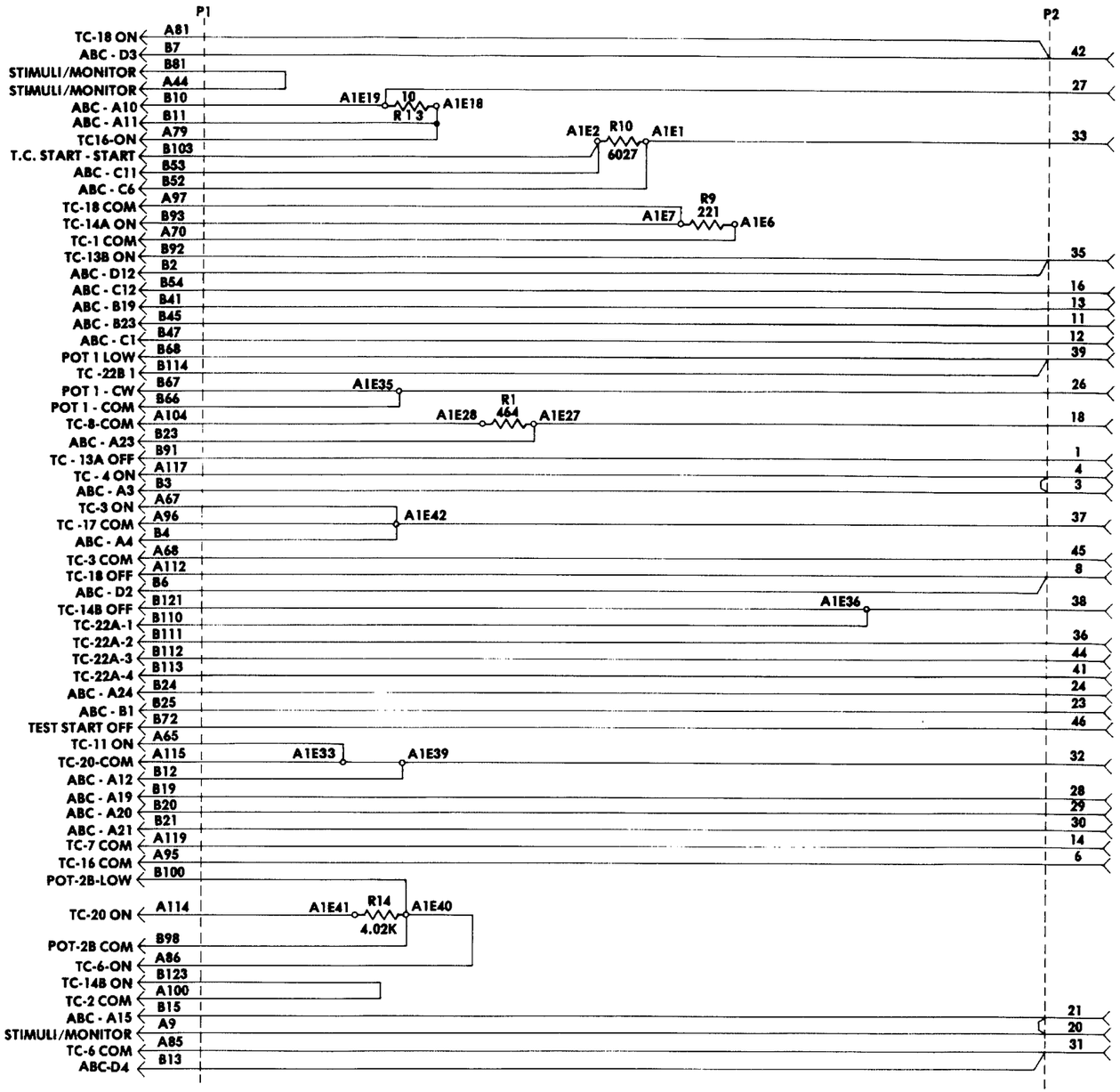
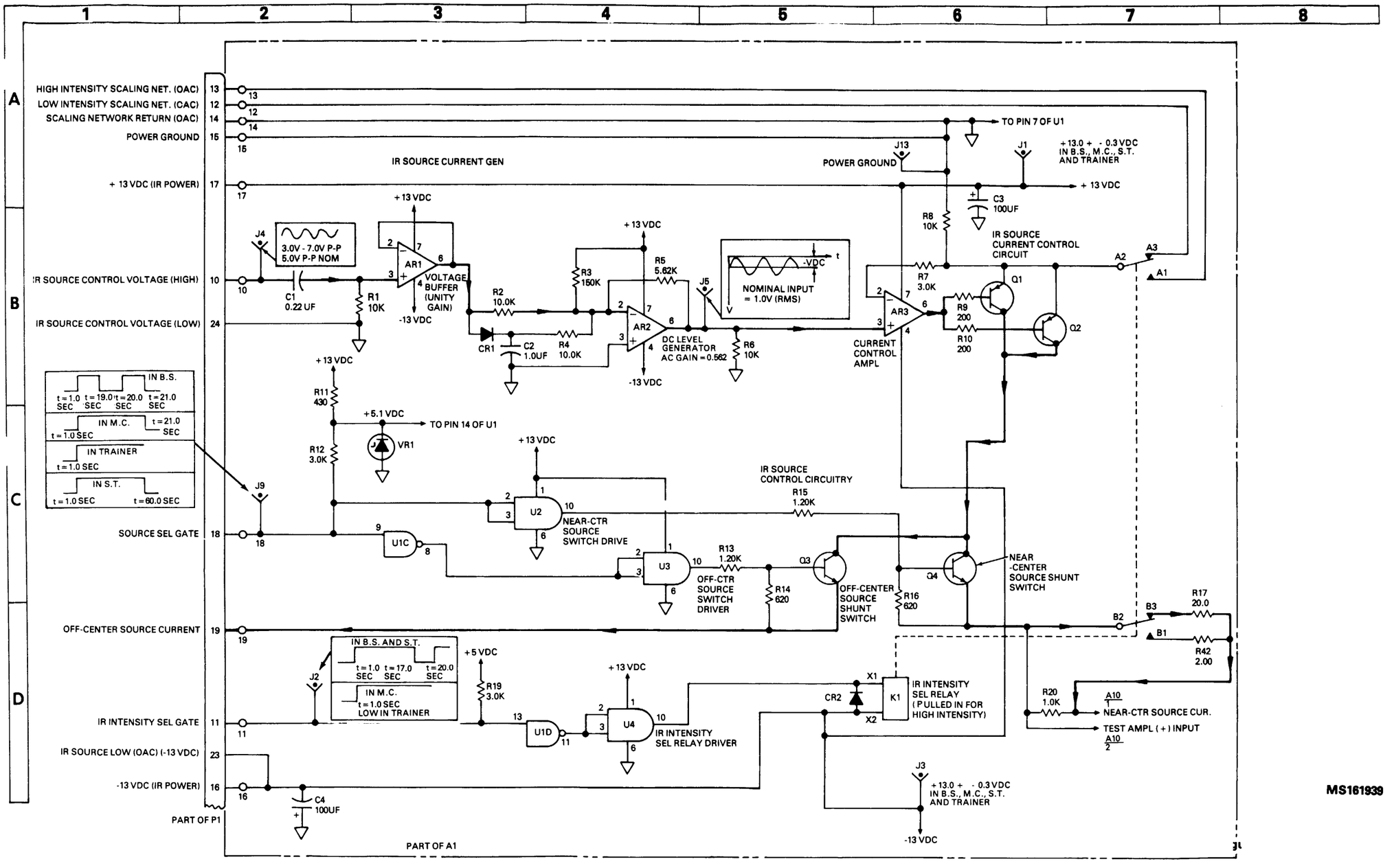


Figure 6-3. A-16 adapter schematic diagram (sheet 1 of 2)



MS161939

Figure 6-3. A-16 adapter schematic diagram (sheet 2 of 2)



MS161939

Figure 6-4. Schematic diagram 1A6A1 (sheet 1 of 2)

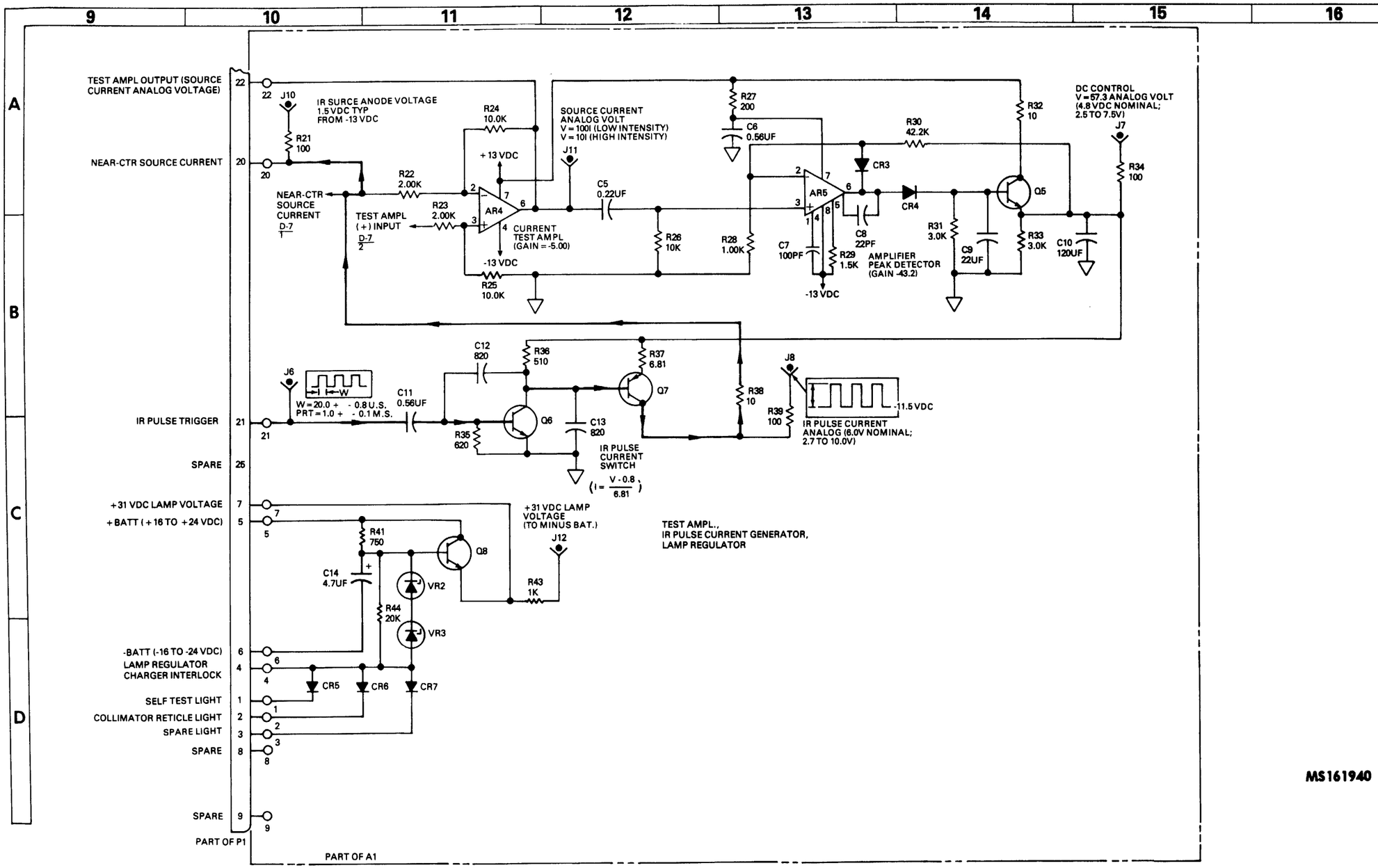


Figure 6-4. Schematic diagram 1A6A1 (sheet 2 of 2)

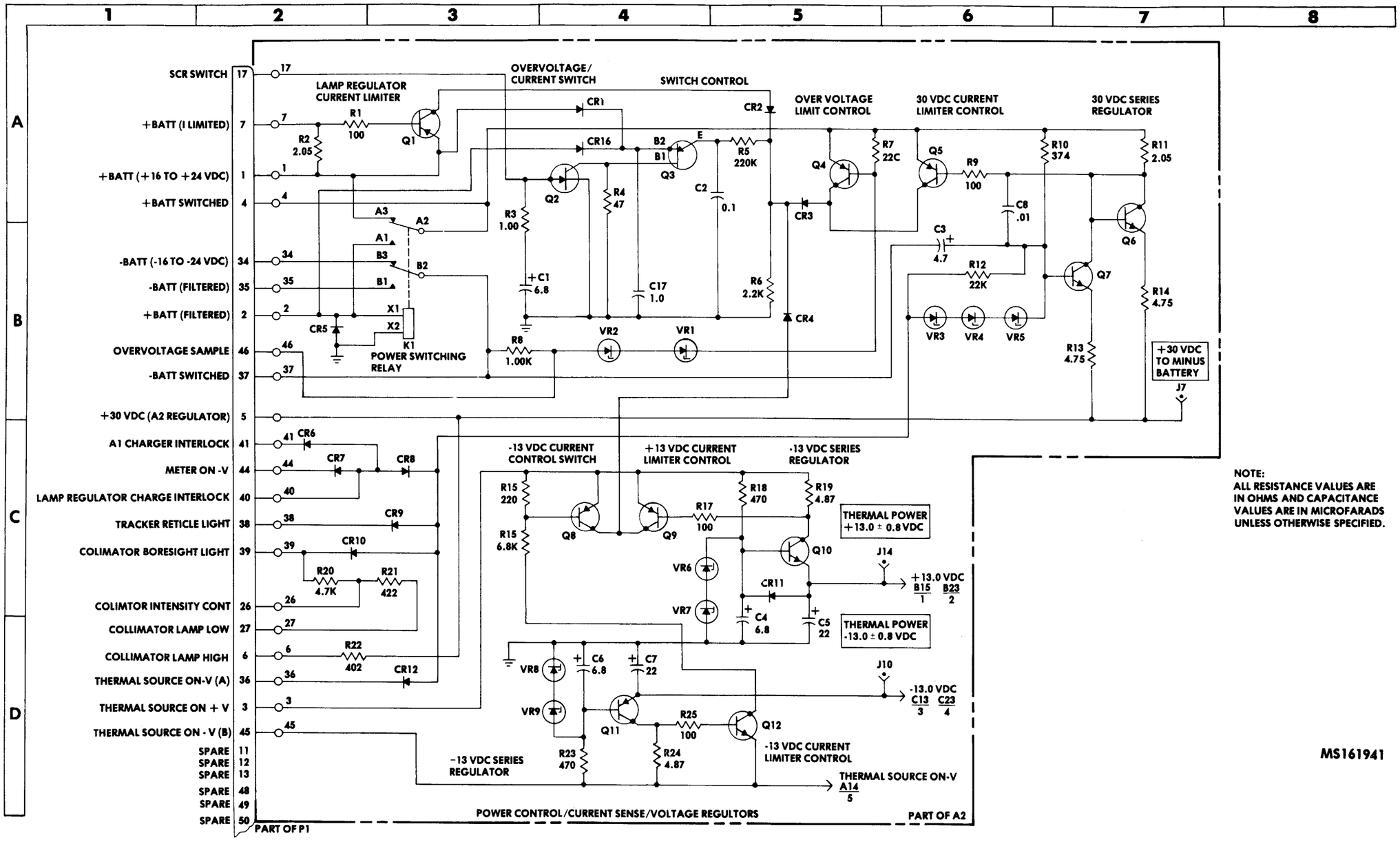


Figure 6-5. 1A6A2 Circuit card schematic diagram(sheet 1 of 3)

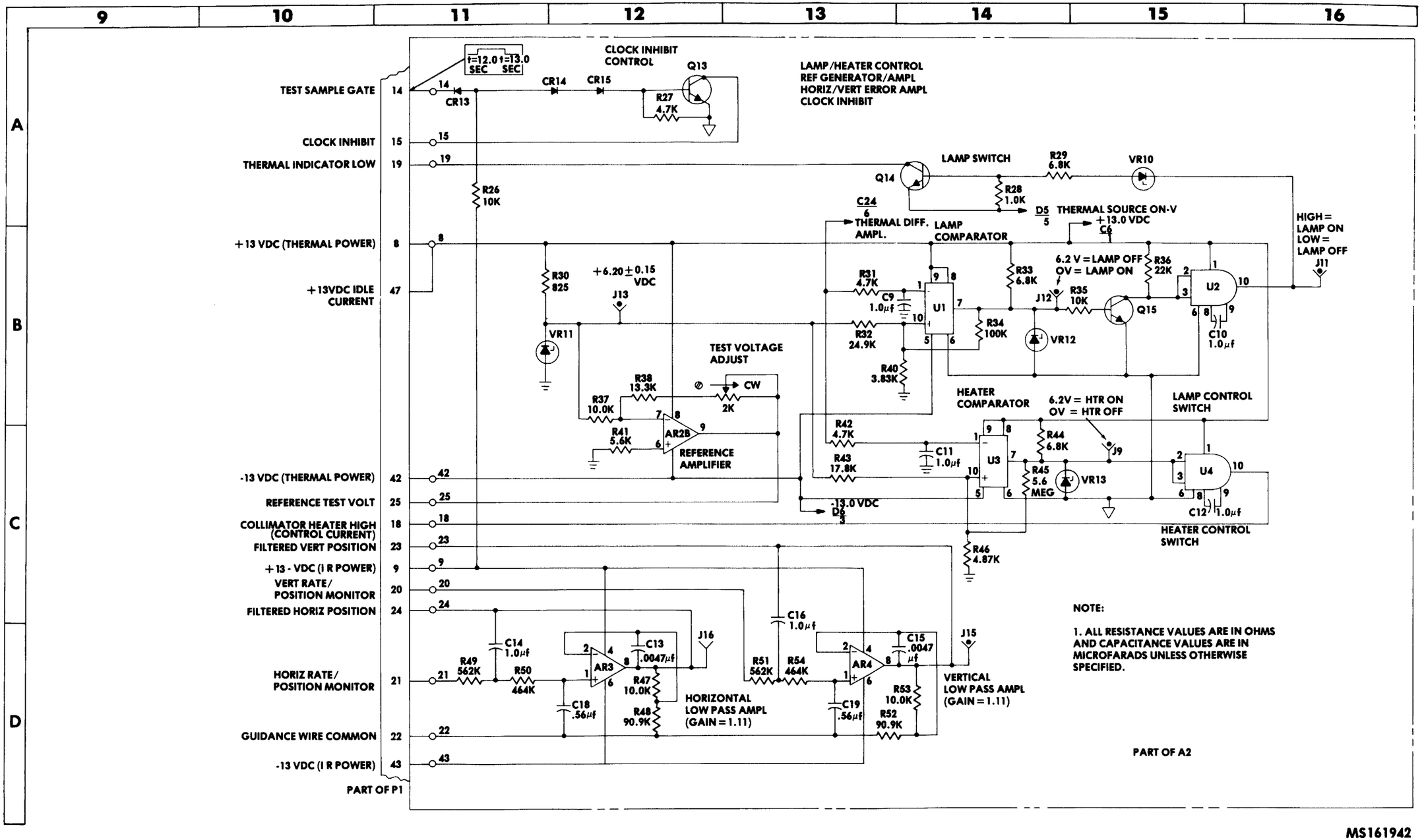


Figure 6-5. 1A6A2 Circuit card schematic diagram(sheet 2 of 3)

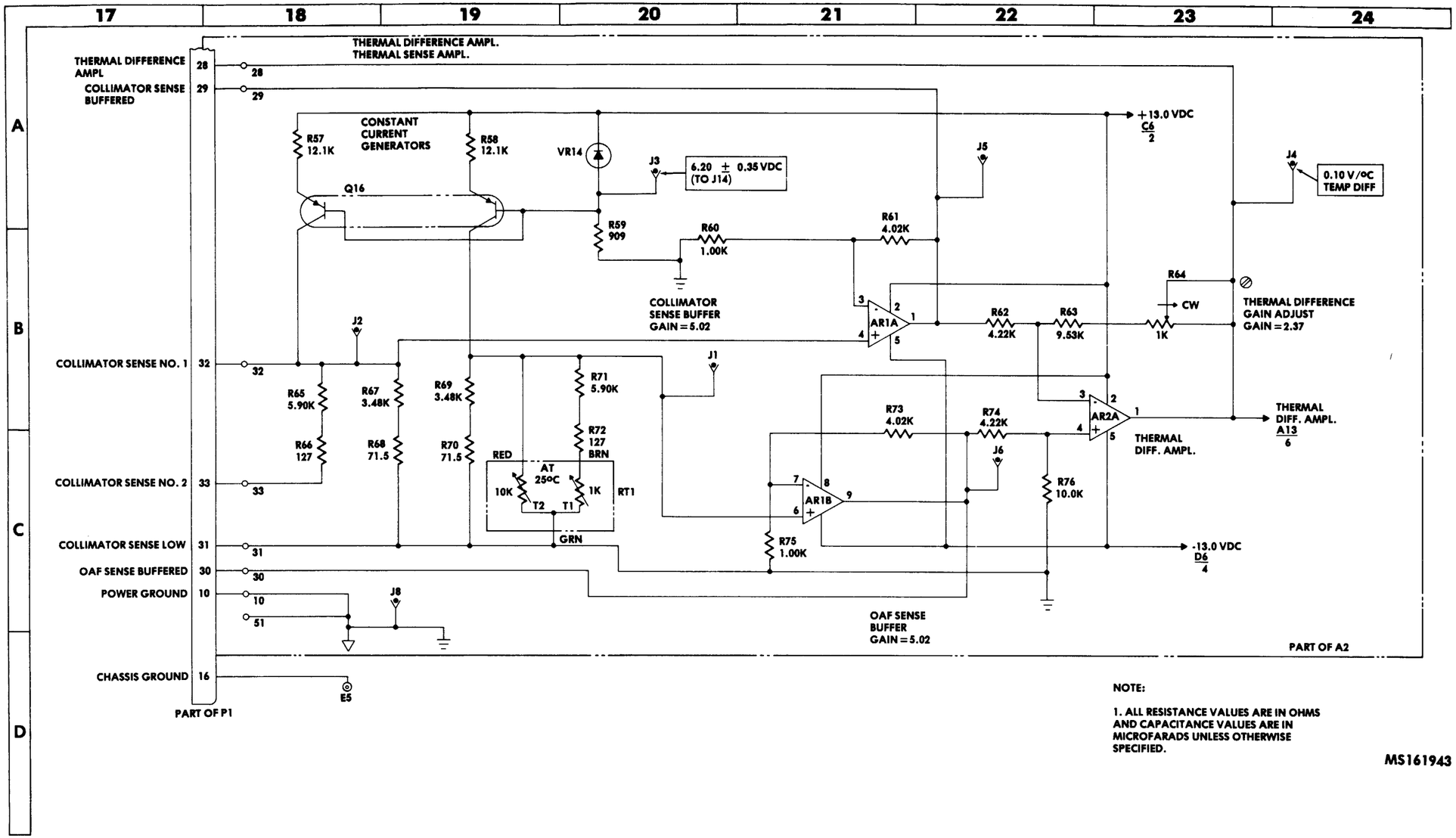
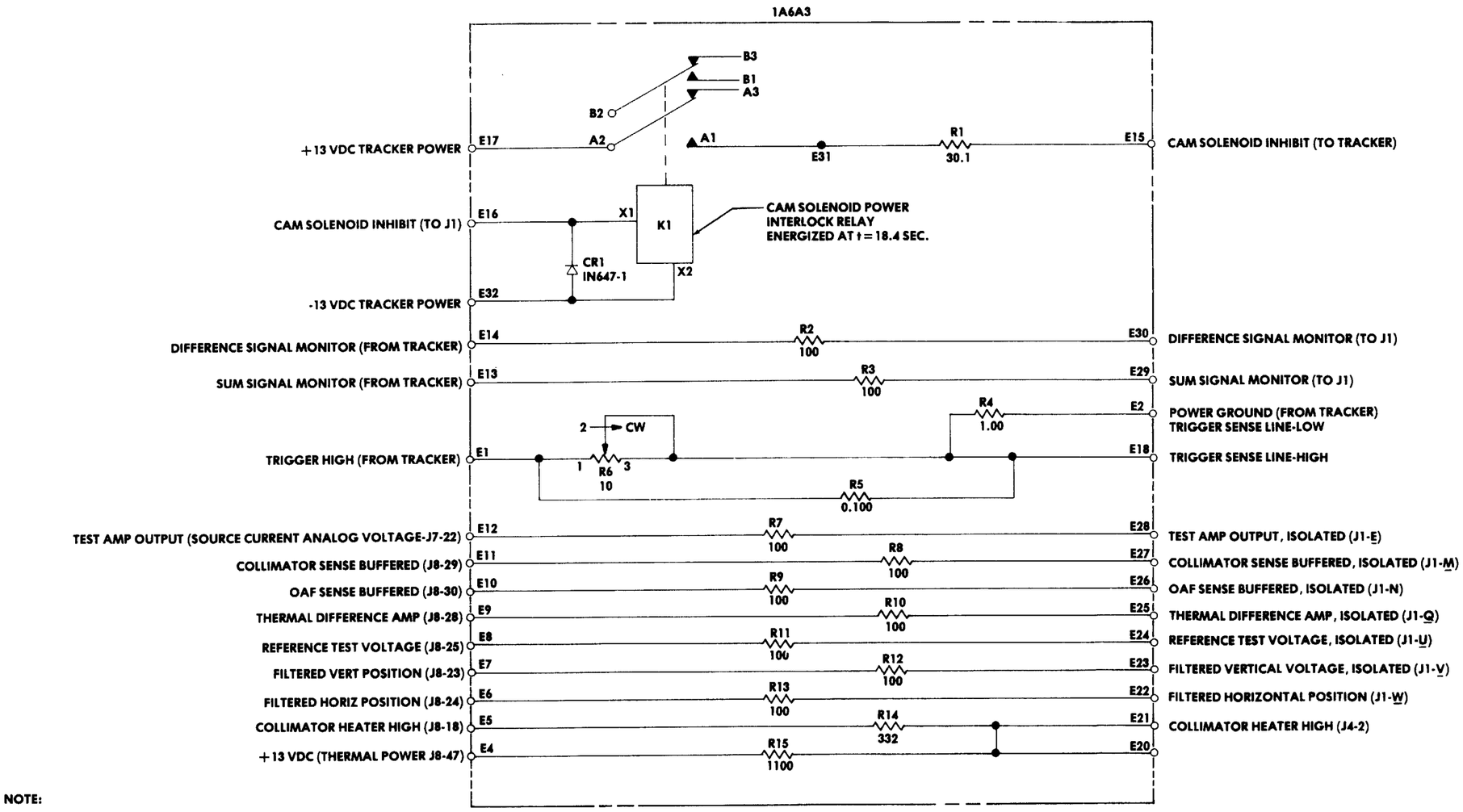


Figure 6-5 1A6A2 Circuit card schematic diagram (sheet 3 of 3)



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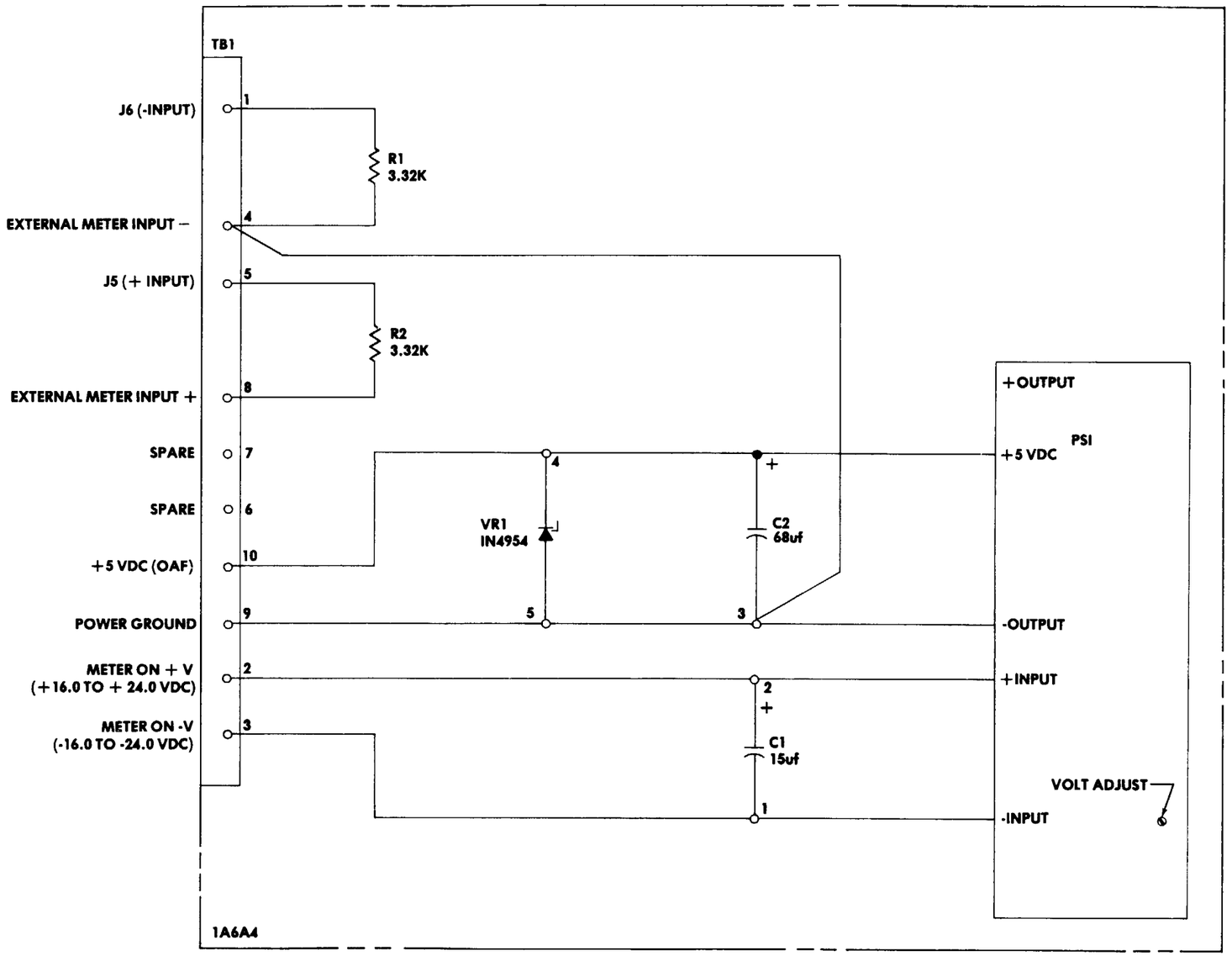
MS161944

Figure 6-6 1A6A3 schematic

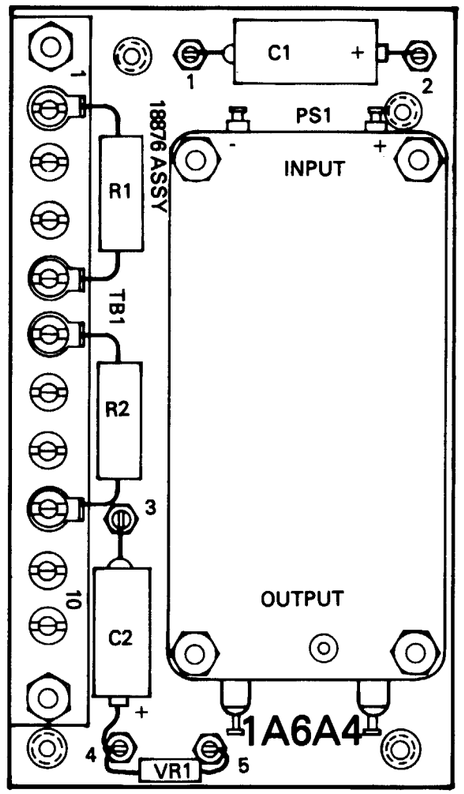


MS161945

NOTE:

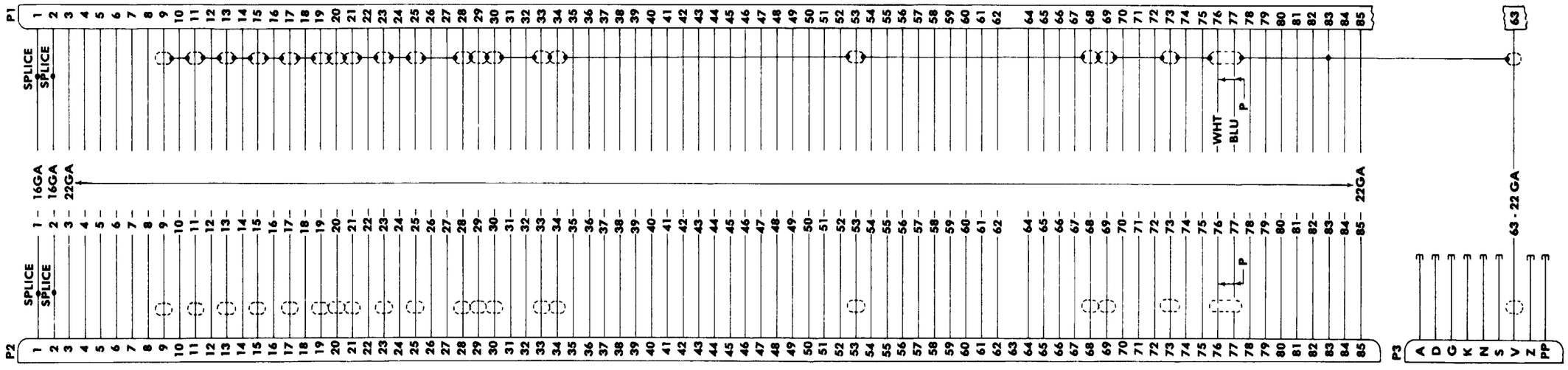
1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

Figure 6-7 1A6A4 Circuit card schematic



MS161933

Figure 6-8 Electronic component assy 1A6A4 parts location



MS161946

Figure 6-9 Special purpose cable -3W1 schematic diagram

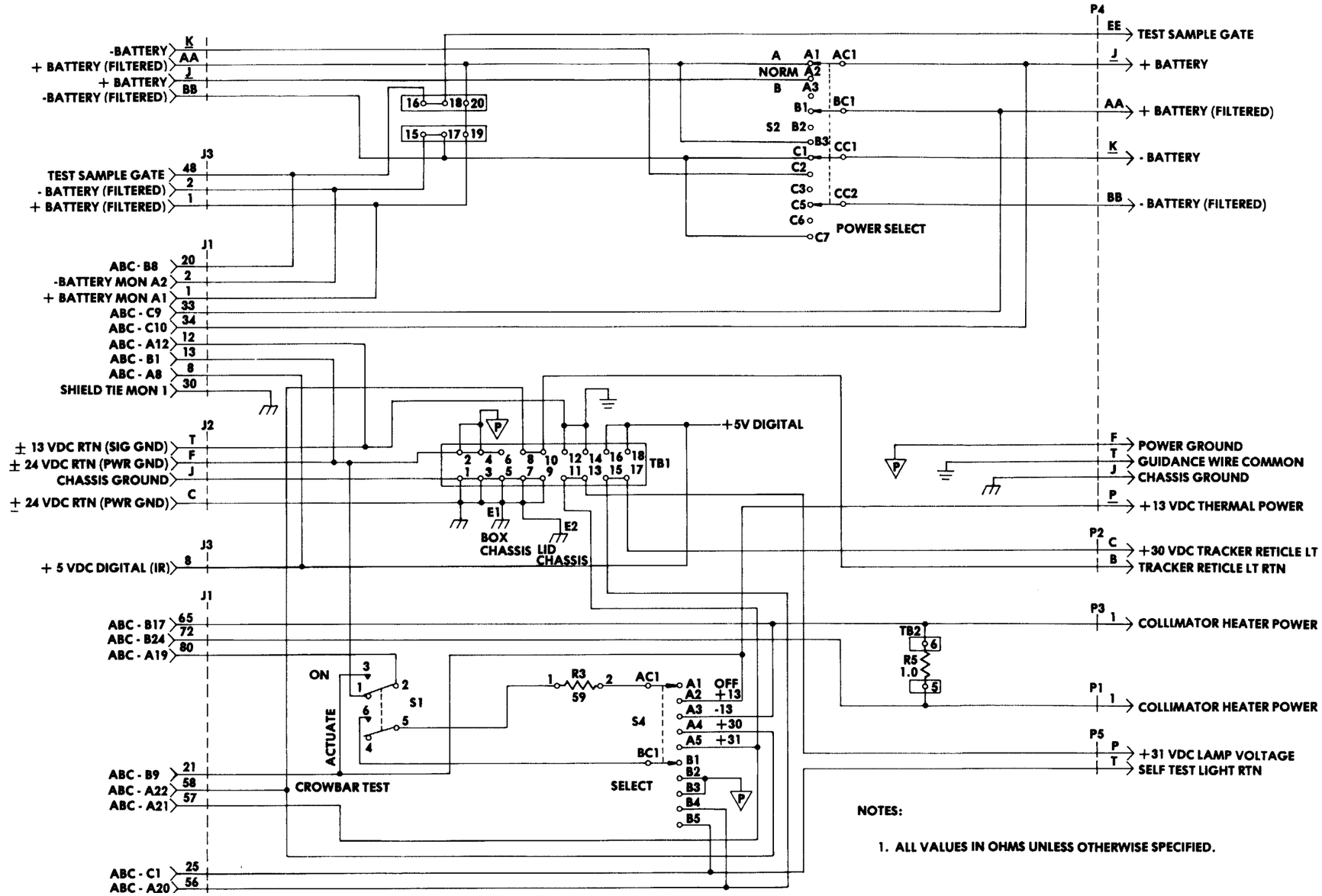


Figure 6-10 Test adapter schematic diagram (sheet 1 of 5)

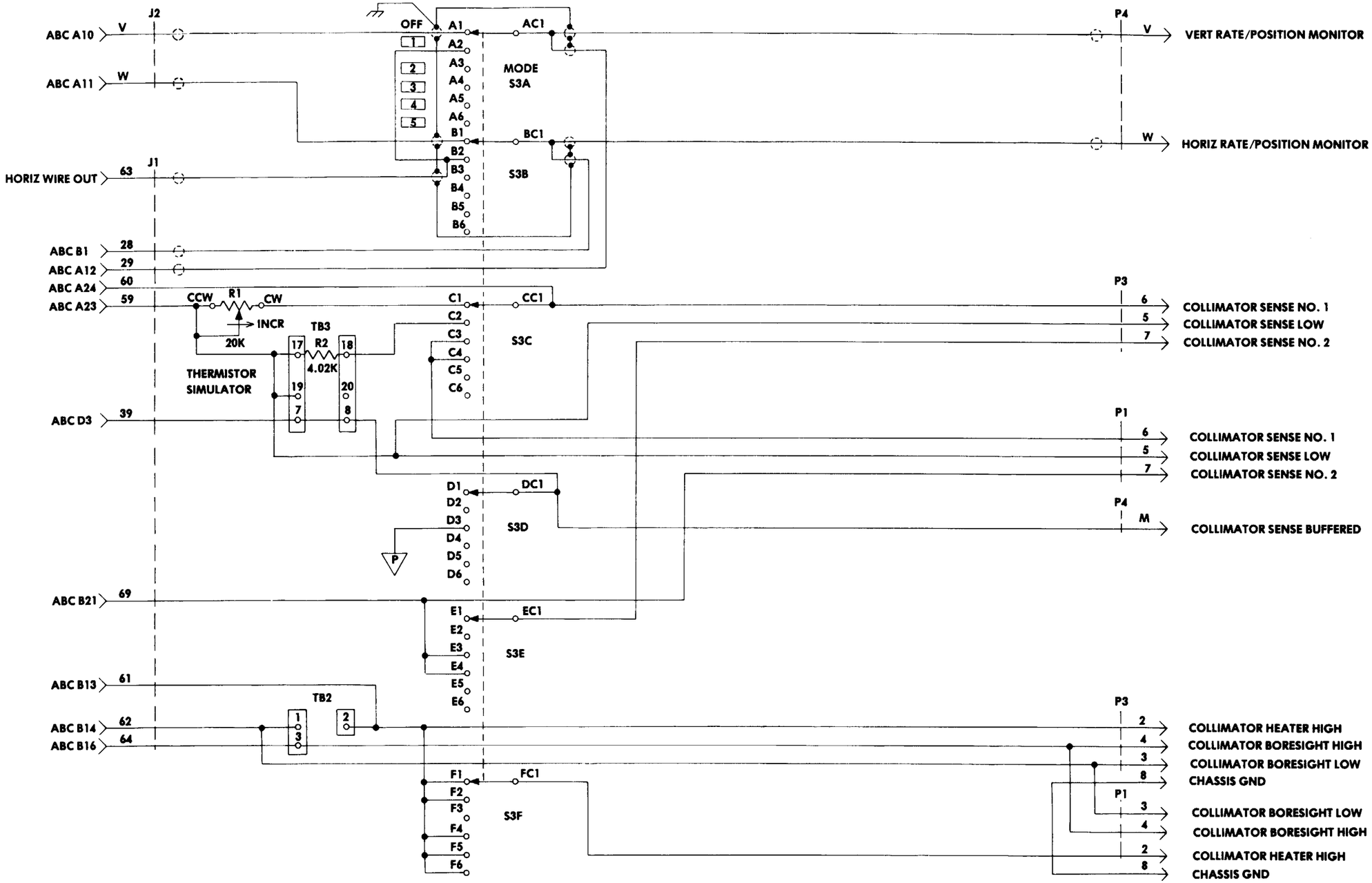
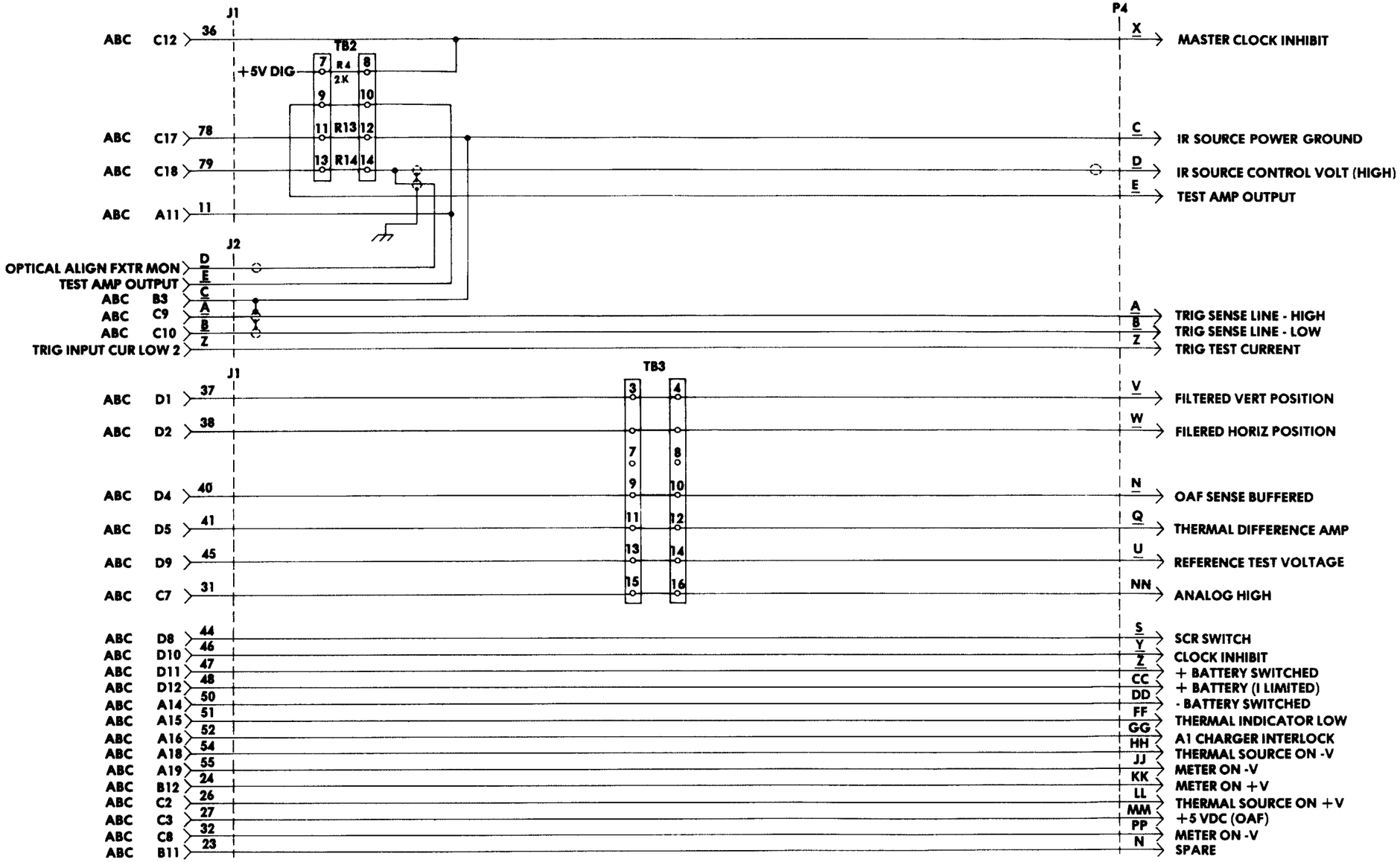
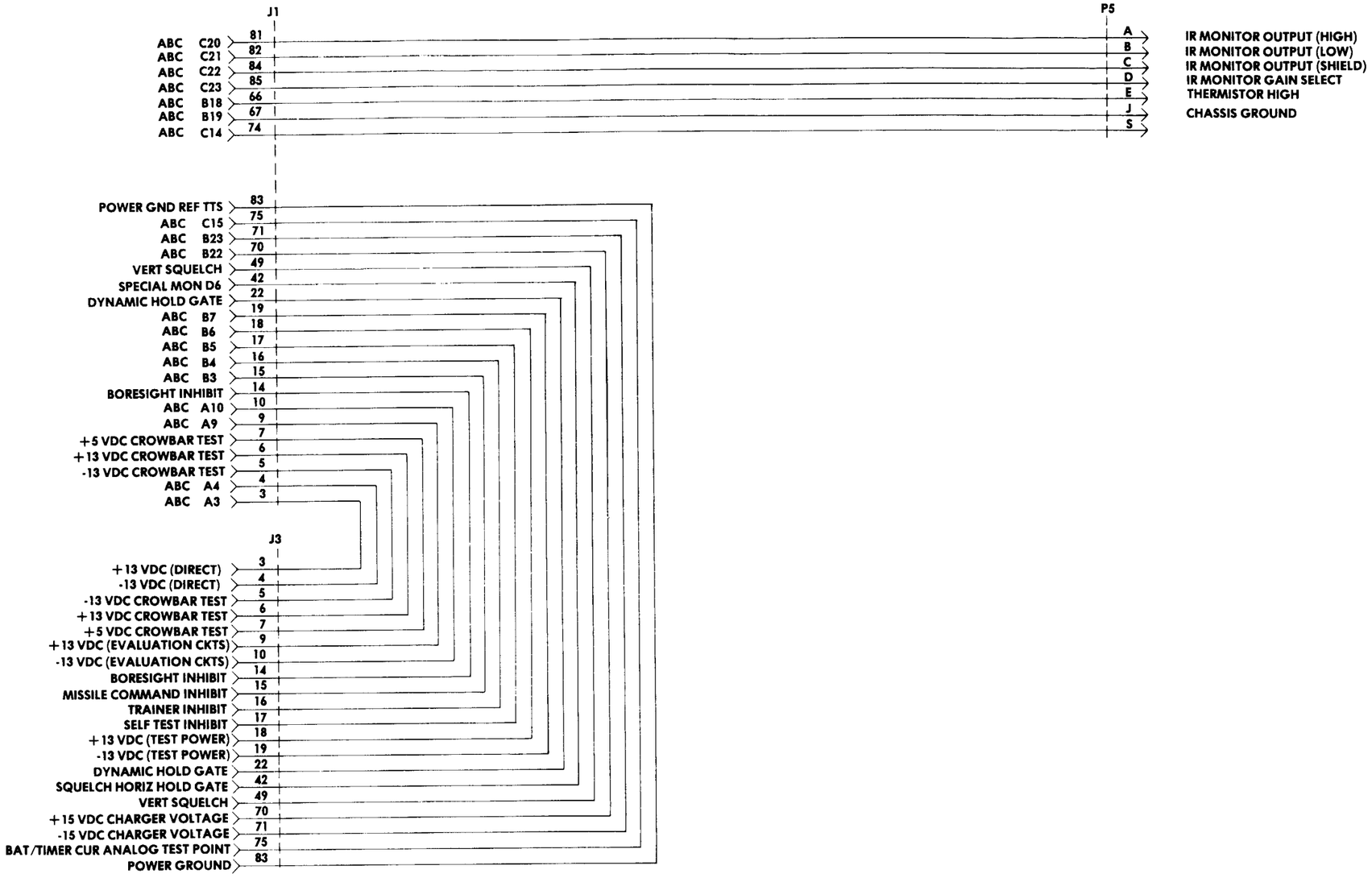


Figure 6-10 Test Adapter schematic diagram (sheet 2 of 5)



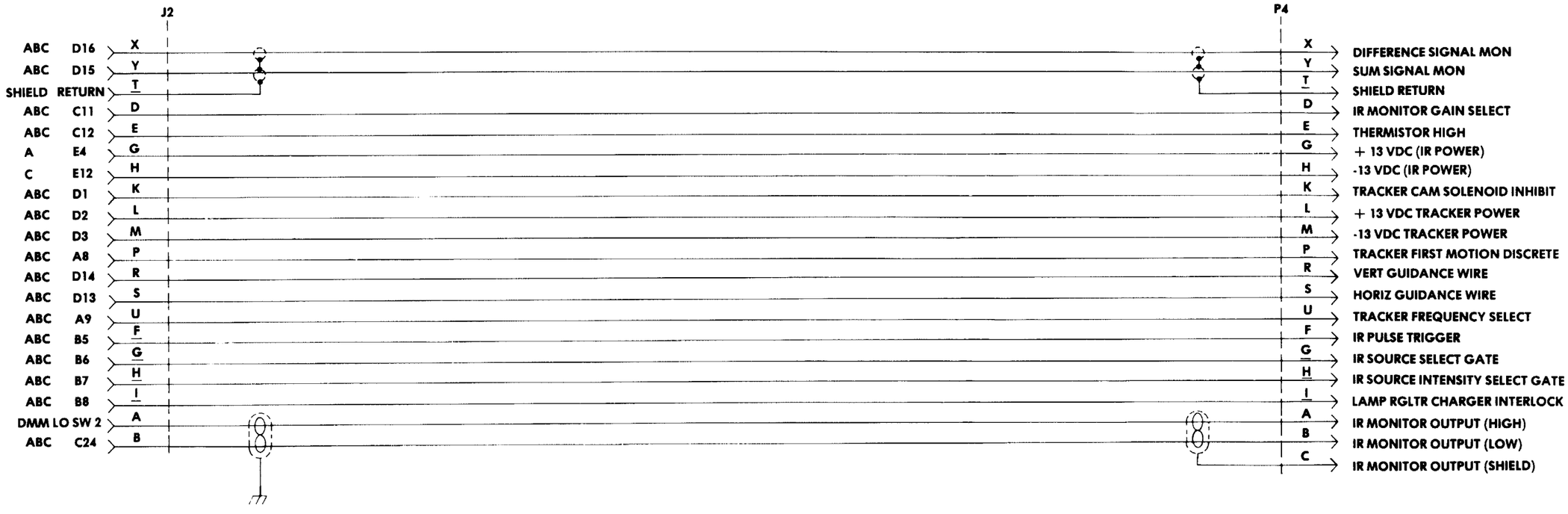
MS161949

Figure 6-10 Test Adapter schematic diagram (sheet 3 of 5)



MS161950

Figure 6-10 Test Adapter schematic diagram (sheet 4 of 5)



MS161951

Figure 6-10 Test adapter schematic (sheet 5 of 5)

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